Letters to the editor

Dear Editor,

I read Ovidiu Popa's article in Vol. 1 with great interest, and also read through the material on his website via the provided link. I admire his energy, relentless quest for improvement, and especially his generosity, even extending to Gerbers for his preamp designs. I suspect he remembers to listen to the music too. Bravo!

I have a few issues, however, with some of the analyses in the article.

The author furnishes a noise analysis of the CCS (constant-current source) in the simplest single-transistor common-base topology, and considers thermal noise in the emitter resistor Re, as well as the transistor's base spreading resistance and noise associated with the equivalent emitter resistance. He concludes that an acceptable approximation of the squared output current noise (per unit bandwidth, assumed throughout hereafter for squared noise quantities) is $4kT/R_e$ --- that is, the preponderance of the noise is due to that resistor's thermal noise. Indeed, although it is not directly stated, that is exactly the expression for resistor thermal noise expressed as a squared noise current.

One omitted term here for the CCS is the shot and excess noise in transistor base current. The minimum squared noise current which appears at the collector is $2q_eI_b$. And typically this noise has a rising low-frequency component, making it of greater significance with RIAA EQ downstream. (1)

Ovidiu Popa replies:
I thank Mr. Wood for reading my article and providing his comments. I will reply to each in the text.
I agree to the above remark. However, the purpose of the entire noise analysis was here clearly oriented at frequencies that are well over the 1/f frequency corner. In a JFET input low noise amplifier, the overall amplifier 1/f corner frequency is, for all practical purposes, defined by the input JFETs and is typically around 100Hz or more. Therefore, any low frequency noise effects originating in the bipolar CCS (usually with 1/f corner frequencies of less than 10Hz) can be ignored by a considerable margin.

The author mentions current noise on his website when describing the device selected as a cascode stage in his HPS 5.1. As well, critical for a CCS, the reference voltage at the base must be sufficiently low noise, and low-enough impedance to make the effect of this noise in I_b negligible.

More curiously though, a remark a few lines later states: "The current noise decreases with the degeneration [meaning R_e] decrease…" However, the equation preceding shows on the face of it that this is upside down --- the current noise from R_e gets smaller with its increase, and we'd like it as large as possible within other constraints (like the available supply voltage and limits on power dissipation).

Thanks for catching this; it should read "The current noise decreases with the degeneration increase…"

But this analysis of CCS noise serves primarily as a preface to the argument that follows, that there is no advantage, for the presented preamp topology, using a CCS in the first place, compared to a simple resistor.

Now no one would dispute that for the same available voltage and required current, the current noise of a resistor is always less than that of a CCS. The transistor(s) always contributes thermal, shot, and excess noise in varying degrees and for proper operation there is some voltage required for a little collector-emitter headroom, which requires the emitter resistor to be even smaller. So why would one wish to use one, ever? Well, to raise impedance and hence gain, and perhaps reduce distortion when the loop is closed. The author argues that, in the location it would have here, there is no advantage because the node it would connect to is a "current-summing" one. This classification evidently stems from the use of U1, an opamp, with feedback resistor Rf, and noting that things connect to its inverting input, which is assumed, we are to suppose, to be at a "virtual ground".

*This is, in principle, entirely correct. However, as also mentioned in the article, the loop gain is defined by g_m*R_F therefore input stage load R_L has virtually no impact on the loop gain. I am only claiming this interesting property (otherwise known since the 60's) for the input stage feeding a virtual ground, so for a combination of transconductance and transimpedance stages. For two voltage gain stages, the use of a CCS load for increasing the loop gain is an obviously good solution, as Brad mentioned.*

But, even granting this approximation that requires the opamp to have large and flat gain with frequency, what about the effect of its equivalent input noise voltage? The author writes: "Interestingly enough, the opamp input noise voltage E_{ni} doesn't contribute much to the total noise budget; there's only a small contribution to the total noise current: $IE_{ni} = E_{ni}/R_L$ ". Well, the expression is about right, and more accurate when R_L includes the JFET output resistance in parallel, and the assessment is certainly true for sufficiently low E_{ni} opamps; in the website discussion and schematic, the OPA211 used for the HPS 5.1 has low voltage noise indeed, at a midband-nominal 1.1nV/rtHz.

I agree that increasing R_L would decrease the E_{ni}/R_L contribution to the current summing node. As such, I am also not advocating that the second stage opamp can have an arbitrary voltage noise performance. What I was trying to argue is that using a low voltage noise like, for example, with E_{ni}=1nV/rtHz and I_{ni}=5pA/rtHz won't cut it here.

But for this article's example, for an equivalent g_m stated as 260mS (8 paralleled BF862 JFETs), a load resistor of 150Ω, a net JFET drains estimated output resistance of 713Ω (open loop with a 1Ω divider R and my BF862 model for 8 paralleled devices) and an opamp with 10nV/rtHz voltage noise, I get, referred to the input, 389pV/rtHz, which is simply $E_{ni}/(g_m'*124Ω)$ (Let's call this net paralleled output/load resistance R_L' from here on out; g_m', 207.4mS, is the reduced transconductance due to the 1Ω). And this is just a midband figure and ignores 1/f noise in E_{ni}. This is anything but negligible when the fundamental limitation on noise should be that of the JFETs.

I haven't directly checked Brad's calculations but, at least as a ballpark, they seem to be correct. I should probably state explicitly, however, that I was nowhere suggesting that a 10nV/rtHz opamp should be used in any implementation targeting an overall noise performance of less than 0.4nV/rtHz. For such, JFET input opamps with E_{ni}=3nV/rtHz and virtually zero I_{ni} are common today, and so are bipolar input opamps with E_{ni}=1nV/rtHz and I_{ni}=1…2pA/rtHz (like the OPA211). These are both appropriate.

But what could the CCS do for us here? The answer is, a whole lot! Even though it will have more than the thermal current noise of the emitter resistor, as mentioned above, it will raise the impedance at that node very significantly, so that it becomes limited by the JFET array's output impedance, and therefore markedly reduce the ability of the opamp E_{ni} to generate noise current.

Agreed, however I would not call this "a lot". I maintain that a CCS is not required for optimal noise performance, neither is it for an increased loop gain, but it always comes (as Brad also mentioned) to a noise penalty. The only advantage I can see in using a CCS is that, indeed, almost all JFET input opamps, disregarding E_{ni}, could then be used.

And we can (and the author does, in the HPS 5.1) raise the node impedance further by inserting, at the JFET drains, a cascaded common-base stage. Hence the CCS can have significant utility. It may contribute a little distortion open-loop due to the variable (2) output impedance with voltage swing, but this will be small given the relatively low voltage swing at that node. The overall improvement in loop gain will almost always entail a net reduction in distortion. And if deemed worth pursuit, better CCS designs exist, with higher output Z and consequently even smaller distortion contributions.

Again, while this is in principle correct, I am not sure it is worth the added complexity to maintain the same noise performance. The purpose of the cascade in HPS 5.1 is mostly to maintain a low Vds for the JFETs, therefore avoiding impact ionization and gate leakage impacts on the noise performance.

By the way, it is unnecessary to invoke the opamp and its feedback resistor for this analysis. Other than from stability considerations (the HPS 5.1 has a 47pF feedback capacitor which is doubtless quite important!), merely having a large gain at that location, when the external feedback loop is closed (in the HPS 5.1 by a 39Ω feedback resistor to the FET sources and the 1Ω feedback divider resistor), entails that the voltage at equilibrium at that node will be relatively small. The feedback resistor is not needed at all. This is as it should be from a noise perspective, as we know that feedback itself never improves signal-to-noise ratio. Thus the "intuition" that the author dismisses in his Conclusions, that increasing the stage gain with a CCS should reduce the second stage contribution to noise, is quite correct --- with or without feedback.

I'm afraid I don't entirely follow the argument here. I thought the loop gain expression is clear, and it does not depend on the first stage R_L. While I agree, as above, that a CCS load will allow an opamp with larger E_{ni} (but lower I_{ni}), I certainly disagree that there is any further real benefit from such a configuration.

R_F can be indeed omitted. The reason for inserting this resistor is simply my preference to work with well defined extrinsic parameters rather than relying, e.g. for the loop gain calculations, on intrinsic device parameters as (here) the opamp open loop gain. The same applies for the loop gain frequency behavior. R_F allows a well defined zero (important for loop stability) in the loop gain.

To conclude this part, I would challenge for a working schematic that would use a CCS for the JFETs, and having improved noise performance. As also mentioned in the article, not only is a CCS always noisier than a simple resistor, but this particular topology DC constraints are also requiring a servo controlling the CCS. It is hard to imagine such a setup without any overall noise penalty, and also hard to justify the extra complexity only for the luxury of using a 10nV/rtHz (or more) opamp.

Moving on to Table 1, "Noise contributors at input node A", an inventory of noise sources at the "current-summing node", the first one labeled InJFET is shown as equal to $4kT*3g_m/2$, in units of A^2/Hz. This term is not correct. (3) The van der Ziel theory of FET thermal channel noise states that the approximate ideal equivalent series noise resistance is $2/(3g_m)$ --- but this fictive noise resistance is merely a means of determining equivalent input voltage noise --- it is not a physical resistance, let alone one generating the current noise of such a resistor as a drain current noise. To determine the actual midband noise in the drain current, it's necessary to multiply the squared input voltage noise, $4kT(2/[3g_m])$, by g_m^2. Thus the proper expression for drain squared current noise becomes $(8/3)kTg_m$.

Correct, and Brad answered his own question: this is for the purpose of calculating the equivalent input voltage noise.

The rest of the entries in Table 1 are correct save the last one. The squared current noise of R_F is simply $4kT/R_F$. The opamp gain has no effect on this, so the A_o term should be deleted. (4)

Not from the current summing node perspective. The R_F contribution is, through the Miller theorem, R_F/A_o in parallel with R_L. I suppose we use different methods to look at the same thing. I prefer to reduce all current noise contribution at the current summing node, then calculate the output voltage noise by multiplying the total current noise by the second stage transimpedance, then calculate the equivalent input voltage noise by dividing the output voltage noise by the loop gain. Brad seems to prefer to add the R_F contribution straight to the output noise.

These terms are combined in equation 9 on the following page and divided by g_m^2 to get the total of squared input-referred voltage noise. Note that the final term in the equation is A_o/R_F. This compounds the error in Table 1 by transposing A_o to the numerator. But A_o should not be involved at all, and if evaluated as shown, that term would overwhelmingly dominate the noise. Let's replace it with $1/R_F$.

No. As above, in my calculations, the RF contribution to the current summing noise is correct.

The rest of the Mr. Wood's calculations are based on his own set of assumptions (regarding R_{μ}, the JFET noise, r0, etc…) which I would, as above, not consider entirely correct. As such, the calculation results can't be better than the assumptions used. There is a simple way to sort this out, just use a variable noise opamp standard model and simulate the entire amp. The contributions of R_L, $E_{n\prime}$, $I_{n\prime}$, R_F will be clearly revealed.

I would though appreciate some details about the quoted r_0=713Ω as the JFET output impedance. Something is not right here, since $r_0=(V_{DS}+1/\lambda)/Id$. I have not seen any specification for Lambda in the BF862 data sheet. But even so, this value is much larger than R_L hence it's contribution to the overall noise (and obviously loop gain) is negligible. R_L is, in HPS 5.1, 100Ω and I would call such a value "typical" for an input stage with 8 paralleled JFETs.

So, given the above amendments, and separating the explicitly thermal noise terms from the others, the expression for the squared input-referred voltage noise should be the sum of:

$(4kT/g_m^2)(2g_m/3 + 1/R_L + 1/R_F)$, the thermal noise terms, and

$(1/ g_{m'}^2)(I_n^2 + E_{ni}^2/R_L'^2)$, the terms arising from the opamp interactions.

On the basis of calculations with the published equation (the A_o/R_F term was presumably not included as such) the conclusion reached in the text is that all of the contributions, following the JFET thermal noise one, are "orders of magnitude lower".

So what do we come up with when the amended expression is used? Well as already mentioned, the squared opamp voltage noise term referred to the input, $(1/g_m{}'^2)\ E_{ni}{}^2/R_L{}'^2$ for the values given is quite significant; taking the square root, estimated at 389pV/rtHz. R_F's contribution is very small, at 1.96pV/rtHz (and can be further reduced by making it a higher resistance, with no disadvantage overall). The thermal noise of R_L itself is a relatively small contribution: referred to the input, 50.66pV/rtHz. The opamp's suggested current noise of 2fA/rtHz in, or $(2fA)^2$ contribution as a squared term, is quite negligible. Here the selection of an opamp should follow the familiar criteria for best performance given the source impedance, in this case R_L. With that rather low value, available bipolar ones will likely be the most suitable. The author is also mindful of the stiff requirement posed by the feedback network on his website discussions, and includes a power buffer after the OPA211 for the HPS 5.1.

With the g_m per device, 32.5mS, given by the author for the BF862 devices, if they follow the van der Ziel theory where the equivalent noise resistance is $2/(3g_m)$, using the corrected expression for drain current noise, and accounting for the g_m reduction and thermal noise of the feedback network of 1Ω input divider and 39Ω feedback with their thermal noise contributions and reduction in input stage equivalent transconductance, the current noise contribution at the drains is $2.52*10^{-21}$ A^2/Hz. That works out to 242pV/rtHz referred to the input. This is actually substantially lower than the contribution from the opamp E_{in} interacting with R_L. Indeed, if it were only upper midband JFET noise to deal with, and followed the ideal theory, and with no feedback network noise, no load resistor (or CCS) noise or second stage noise, and the chip temperatures held close to 300°K, the input voltage noise spectral density would be only 206pV/rtHz at room temperature (this for the 8 paralleled FETs). Wurcer (5) finds the BF862 at 1mA Id to even slightly better the van der Ziel theory, although I suspect this is unlikely to hold up at high drain currents.

Fully cranked through, I get a predicted equivalent input voltage-noise spectral density of 461pV/rtHz. We are done in here by the opamp voltage noise and the low value of resistance at its input. The HPS 5.1 avoids this pitfall by using a much lower input voltage noise opamp.

Another issue: the author attempts to address the suggestion advanced by Gerhard in Vol. 0, that there is some sort of mysterious thermodynamic limit that prevents much further improvement in preamp performance, "the apparent 'saturation'…" near 300pV/rtHz. One explanation offered is that we can't make the load resistor arbitrarily high in value. But this presumes a limitation on the positive supply rail, and whereas this may in many cases be a good practical consideration, one cannot

consider it anything fundamental, the author's concerns about JFET breakdown voltage and power dissipation notwithstanding (provide a clamp for excess voltage if necessary, and use more and higher-rated resistors!).

I agree, theoretically this can easily be addressed by an arbitrary large supply voltage, there is no fundamental theoretical limitation for that, and I think I mentioned this in the article. I was trying to keep the analysis in the frame of practicality, though. Certainly nobody would appreciate a 10W (or even more) resistor on the low noise amplifier PCB. As a side note, even with a R_L=100Ω dissipating slightly under 1W, I have my Inbox full of worried emails about "overheating", coming from HPS 5.1 builders.

And emphasizing the concern that higher temperatures increase thermal noise is perhaps somewhat misleading, for both resistors and JFETs, as thermal voltage/current noise spectral density goes as the square root of absolute temperature --- going from 300° to 400° K only represents about a 15% increase in JFET en or resistor in --- not welcome, but not devastating. There can be increases in excess noise in the presence of significant thermal gradients, and of course drain-gate leakage goes up, usually doubling for every 10°K increase --- so cooler and more uniform are better, to a point. Leakage current in particular is not much of a limitation here, for these source impedances. (6)

15% is indeed not "devastating" but I would also hardly ignore it. When one designs for 0.4nV/rtHz or less, every bit counts. But otherwise, interesting enough, exactly this kind of reasoning made me abandon a Peltier cooled low noise amp project; the complexity of cooling to -100C (or less), while avoiding water condensation, for a 20% noise reduction premium, is certainly not worth the trouble for any audio applications. I'll leave such a project for those astronomy hobbyists interested in low noise CCD sensors for telescopes.

The remark following about the value of a bipolar cascode stage after the JFETs is good advice. Although advanced to reduce JFET drain voltage and hence dissipation, and allow the voltage swing at the collector to be just limited by the bipolar breakdown voltage (if permitted by the opamp stage), an additional benefit as mentioned above is the increase in nodal output impedance. As noted, such a stage is used in the HPS 5.1. In that supporting material it is mentioned that the selected device has beta >400 and thus contributes little noise (this is the same noise discussed above, due to base current shot and excess noise, as important here as for a CCS). But then we read that "Being a common base circuit, the bipolar cascode noise contribution is small, therefore there's no need to use an ultra low noise transistor. Almost any medium power device will do just fine." Well, indeed, voltage noise is almost immaterial, since the source impedance feeding the emitter is the paralleled JFET drain impedance (7); but the device should still have high beta at the required collector current. And it helps if it has a high gain-bandwidth product, so that the added parasitic pole is at a high frequency. A DMOS part could be considered, but will require considerably more voltage to function properly, pretty much ruling it out for a +18V rail and an opamp second stage.

I fully agree; these are all good points.

Note that none of the above leads me to doubt the excellence of, and the veracity of the measurements on, the author's HPS 5.1 head amp! I am very glad I did read that material, and I greatly appreciated the account of the history of the development and the design decisions made. I hope these remarks are found to be helpful and constructive.
I am grateful to Samuel Groner for reviewing this letter, and offering suggestions and references. Any remaining mistakes and unbridled verbosities are entirely my own responsibility.

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Notes and references:

(1) Bowers presents a brief analysis of a simple CCS in "Minimizing Noise in Analog Bipolar Circuit Design", in Proceedings of the IEEE 1989 Bipolar Circuits and Technology Meeting, pp. 107-111.

(2) And nonlinearly variable, but it generates distortion even if it varies linearly.

(3) See for example: http://users.ece.gatech.edu/mleach/ece6416/Labs/exp05.pdf

(4) A flat open-loop gain will reduce the inverting input's resistance due to R_F, making things appear as if there is a resistor there to a.c. common (or what the noninverting input is tied to) of value $R_F/(A_o + 1)$. Since the physical resistor still has the smaller current noise of its physical value, if the opamp input voltage noise and current noise are sufficiently low, the circuit can behave like the smaller resistor but with lower-than-thermal noise current (note that this lower resistance does not appear as a paralleled value with R_L for noise considerations). This is an example of a so-called synthetic "cooled termination", and the concept goes way back to pre-transistor times. As applied to lower-noise MM cartridge loading, it's discussed in Douglas Self's excellent recent book, Small Signal Audio Design (ISBN 978-0-240-52177-0). See pp. 197-201. (Reviewed in Linear Audio Vol 0 – ed).

(5) Wurcer, Scott, "Low Noise Microphone Preamplifiers", Linear Audio Vol. 1, p. 105

(6) Actually, for a no-holds-barred design, a regulated cooling system is not a bad idea, not only due to the opportunity for slightly-reduced thermal noise, but because some of the higher-temperature-coefficient parts of the circuits, especially the JFETs, could benefit from better temperature stability, to reduce low-frequency fluctuations that the d.c. servo may otherwise struggle to keep up with. Servoed Peltier devices with local temperature sensor feedback are straightforward, at least in principle. They are rather inefficient, but why should only the tube aficionados have all the fun

squandering energy, anyway?

(7) Although beware of the drain-source voltage getting too small, and this impedance getting smaller with it; as mentioned above my BF862 model predicts 713Ω for 8 paralleled devices with Vds about 6V, which is a pretty low resistance already. And according to Wurcer in (5), it may be well to keep V_{ds} below 5V for these parts --- although for his condenser mic application, he's quite properly more concerned, by far, with gate leakage.