Low Input Impedance Current-to-Voltage Conversion Circuit for Current-Output Digital-to-Analog Converters 4326 (B-1)

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Low Input Impedance Current-to-Voltage Conversion Circuit for Current-Output Digital-to-Analog Converters

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A low input impedance current to voltage conversion circuit for use with current-output digital to analog converters is described and analyzed. The performance is compared with traditional approaches, which include circuits based on integrated operational amplifiers. PSpice circuit simulations show the performance differences between these circuits.

1 Introduction

One-bit digital to analog converters (DAC's) have become increasingly popular due to their inherently good low level linearity. However, the multibit approach has a potential for better performance than the one-bit approach due to the differences in basic working principles of these DAC architectures. Since the one-bit DAC relies heavily on noise shaping to achieve good performance in the audio band, the large amounts of out-of-band noise can affect the audio performance through intermodulation effects. Another problem associated with one-bit DAC's is the possible generation of idle tones caused by partial correlation of the quantization noise. In [3], one example of a high-performance multibit architecture is presented and compared to other approaches, and the particular advantages of the multibit approach are discussed. In [4], a method for linearization of a multibit DAC is presented, and the authors have here been able to achieve 20 bit linearity from a 16 bit DAC. Multibit converters have due to their resistor ladder architecture a current output. A critical point in maximizing the performance of a multibit DAC is the current to voltage (I/V) conversion stage. This stage must ideally have zero ohms input impedance (Z_{in}) independent of frequency and infinite bandwidth in order to convert the non-filtered DAC output current into an equivalent voltage without adding distortion to the signal. Especially when reproduction systems with higher word lengths than the current 16 bit set by the Compact Disc standard become widespread, digital to analog conversion with higher accuracy than today will be needed.

1.1 The Multibit DAC Topology

In a multibit DAC, the digital n-bit input code controls n switches that each connects a binary weighted current source to a common output summing node. In figure 1, a 16 bit example of the most common circuit topology for this type of converter is shown; the R-2R ladder topology. The shunt resistors all have the value 2R, and the series resistors all have the value R. At the endpoint, the ladder is terminated with a resistor of value 2R. A reference voltage V_{ref} connects to the left end of the ladder, and each shunt resistor is either switched to ground or the current output pin I_{out}, which is assumed to be a virtual ground node. The current flowing through shunt resistance n is twice the current flowing through shunt resistance n-1, providing the required binary relationship between the current sources.
If $Z_{in}=0$, I_{out} for the n-bit R-2R ladder topology is:

$$I_{out} = \frac{V_{ref}}{R} \sum_{i=0}^{n-1} \frac{D_i}{2^{n-i}}$$

where D_i are the databits.

1.2 I/V Converter Requirements

It is obvious from figure 1 that it is important that the I_{out} output actually is kept at ground potential. If Z_{in} of the following I/V converter is not zero, then the resulting output current will not have the correct value. Of course, a small static value will not have the same effect on signal quality as a Z_{in} that is code/frequency dependent.
The I/V converter should fulfill the following requirements:

- Z_{in} should be as low as possible.
- Z_{in} should be constant not only in the audio band, but up to frequencies where the DAC output current no longer has any significant spectral content. Remember that the DAC output current is staircase-shaped with the steps separated by a sample interval, and most multibit converters use oversampling filters. In other words, the I/V converter must be able to handle the significant high frequency content of the DAC output current without creating any audible artifacts.

2 Commonly Used I/V Conversion Circuits

A number of different I/V conversion circuits exist, but it is beyond the scope of this paper to describe all variants. The circuits mentioned in this section based on integrated operational amplifiers (opamps) cover most applications today.

2.1 Opamp With Voltage Feedback

Figure 2 shows a circuit based on a voltage feedback opamp. The output voltage is:

$$V_{out} = -I_{DAC} R_1$$

This circuit is simulated using a particular high speed precision opamp with a slew rate of 100V/µs. Fig. 3 shows the transient response with R_1=1kΩ. Under- and overshoot is clearly visible. The frequency response in fig. 4 shows a +10dB peak at 22MHz. The input impedance has a maximum value of more than 3000Ω at the same frequency, as shown in fig. 5. Much more serious is however that the input impedance increases from 4mΩ at 10Hz to 1Ω at 20kHz to 52Ω at 1MHz. The input impedance from 10Hz to 100kHz is shown in fig. 6. In most applications, the I/V

converter stage has a lowpass filter function as shown in fig. 7. C_1 forms a pole together with R_1. The -3dB cutoff frequency has been selected to 50kHz. Again, R_1=1kΩ. The input impedance is the same in the audio band as without C_1, but at 1MHz it is now 2.7Ω compared to the 52Ω we had before. At 10MHz and 100MHz where the opamp's feedback is not able to maintain a low input impedance, the capacitor lowers the input impedance considerably. This can be seen in fig. 9.

2.2 Opamp With Current Feedback

Current feedback opamps have some interesting performance attributes that make them interesting for applications where high slew rate and bandwidth are desired. Fig. 11 shows an I/V converter using a current feedback (or transimpedance) opamp. The output voltage follows the same equation as for the voltage feedback amplifier. This circuit is simulated using a particular high speed opamp with a slew rate of 2500V/µs. Again, R1 is set to 1kΩ. The transient response in fig. 12 is very fast and with only little undershoot. The input impedance (fig. 14 - 15) rises from 9.5mΩ at 10Hz to 12mΩ at 20kHz. In opposition to the voltage feedback amplifier, the current feedback opamp is able to maintain a reasonably low input impedance at very high frequencies due to more efficient feedback. At 1MHz, the input impedance is 348mΩ, rising to 3.5Ω at 10MHz and 40Ω at 100MHz.
Since most applications call for a pole in the I/V conversion stage, the circuit will then be like shown in fig. 16. This is identical to the circuit of fig. 7 apart from R_2. Since the feedback resistor R_1 for a transimpedance amplifier also serves as an element of the frequency compensation network together with an internal capacitor, it can not be chosen freely. The feedback resistance determines the closed loop bandwidth. If it becomes too small the amplifier will become unstable. To avoid this it has been suggested in [5] to add the 1kΩ resistor R_2 to the circuit. However, this has performance implications as we will see from the simulations. Input impedance is now increased by a factor of 70 in the audio band, and there are no significant benefits outside the audio band. This is shown in fig. 18 and 19.

3 The Current Conveyor Approach

In stead of using an opamp that relies on global feedback, other topologies have been suggested for the I/V conversion stage. One of them is the current conveyor. A current conveyor conveys the input current unaltered to the output, but with different impedance levels. The input impedance is very low (ideally zero ohms) and the output impedance is very high - typically several megaohms. An example of such a current conveyor circuit has been described in [1]. The input impedance of this circuit was reported to be 2Ω. The frequency dependence was not discussed.
Before going to performance analysis of the current conveyor circuits, it is worth to consider the nature of the signals being processed. In particular, the hold function of a multibit DAC has an interesting filtering effect on the output current. The hold effect occurs when a digital input value is converted to an output current level. This current level is then held until the next sample occurs.
The frequency-dependent attenuation A(f) resulting from the hold function is given by the following formula:

$$A(f) = \frac{SIN\left(\frac{f\pi}{f_s}\right)}{\frac{f\pi}{f_s}}$$

Where f_s is the sampling frequency.
In fig. 20 - 23 this function is evaluated for a sampling frequency of 352.8kHz, which corresponds to the common value of 8 times oversampling from 44.1kHz. In fig. 22 it can be seen that around 352.8kHz the mirror images of the audio signal are attenuated at least 24dB, and at higher frequencies the mirror images are attenuated even more. This reduces the requirements for lowpass filtering after the DAC, and in some applications a simple first order lowpass filter will be sufficient. For example if two or more DAC's are operating time-interleaved and their output currents are summed, this configuration alone will lowpass-filter the signal. Such a configuration essentially is an analog implementation of a lowpass FIR filter. In such a case, a first order lowpass filter is sufficient. (As it can be seen from fig. 23, the attenuation in the audio band resulting from the hold function is lower than 0.05dB, and should not be audible. Some oversampling filters employ equalizing to eliminate this attenuation in the audio band.)
Because of the above considerations, a new circuit topology with scaleable multiple input nodes has been developed. In this paper, only the variations with two input nodes will be discussed. All examined input impedances are for one node only.

3.1 Dual Input Current Conveyor

The first iteration of the circuit is shown in fig. 24. The input stage consists of a dual grounded base section, and the input currents are conveyed to and summed at the buffer output stage that forms a high-impedance output. This means that a simple resistor can be used for the current to voltage conversion. All following simulations use a 1kΩ resistor. A first order lowpass reconstruction filter can be implemented by paralleling this resistor with a capacitor as shown in fig. 24. Using multiple multibit DAC's, this is in most cases sufficient to attenuate the out of band energy. For the simulations however, only a very small C_1 was used in order to achieve a clean transient response. Contrary to the opamp topologies, this single pole does not affect the input impedance. A simpler variation of the circuit in fig. 24 is made by removing Q_3, Q_4, I_1 and I_2. The circuit is then basically a symmetrical version of the widely used grounded base circuit. The input impedance is then similar to the circuit in fig. 24, but distortion is not quite as good because of the absence of a circuit that feeds the base currents back into the signal path, so this derivative will not be examined. The transient response is shown in fig. 25, and there is no under- or overshoot. The rise time is determined by C_1. The input impedance is 2.5Ω from 10Hz up to 3MHz as shown in fig. 27 and 28. At 10MHz the input impedance level is 3.1Ω, rising to 21Ω at 100MHz. The input impedance is very flat compared to the opamp approaches.

3.2 Current Conveyor With Complementary Compound Input Stage

In order to lower the input impedance, the input section has been replaced by a dual complementary compound section biased by resistors as shown in fig. 29. This way, Q_6 and Q_5 which determine the input impedance level operate with nearly constant current, while Q_3 and Q_4 convey the DAC current to the output stage. The transient response has not changed as fig. 30 shows, but input impedance is now 112mΩ

from 10Hz to 600kHz, rising to 115mΩ at 1MHz, 143mΩ at 3MHz, 395mΩ at 10MHz and 21Ω at 100MHz. The input impedance curves are shown in fig. 32 and 33.

3.3 Current Conveyor With Active Biased Complementary Compound Input Stage

In order to lower the input impedance further, the dual complementary compound input section is now biased by active current sources and sinks as shown in fig. 34. This biasing scheme prevents Q_3 and Q_4 from modulating the currents in Q_6 and Q_5, respectively. The transient response has not changed as fig. 35 shows, but input impedance is now down to 7.0mΩ from 10Hz to 50kHz, rising to 7.4mΩ at 100kHz, 79mΩ at 3MHz, 321mΩ at 10MHz and 21Ω at 100MHz. The input impedance curves are shown in fig. 37 and 38.

3.4 Current Conveyor With Active Biased Complementary Compound Input And Output Stages

In order to lower the input impedance even further, the output section also has been replaced by a dual complementary compound section biased by active current sources and sinks as shown in fig. 39. This reduces voltage modulations on transistors Q_3 and Q_4, hence Q_6 and Q_5. Once again, the transient response has not changed as fig. 40 shows, but input impedance is now down to 6.7mΩ from 10Hz to 40kHz, rising to 7.1mΩ at 100kHz, 74mΩ at 3MHz, 312mΩ at 10MHz and 21Ω at 100MHz. The input impedance curves are shown in fig. 42 and 43. Bandwidth has also increased a bit by this modification as shown in fig. 41.

Table 1 summarizes the performance differences between the examined I/V converters. It should be clear by now that the current conveyor approach offers a new performance level for the I/V conversion stage.

4 Conclusion

Contrary to I/V converters based on integrated operational amplifiers (opamps), current conveyors offer a constant input impedance in and above the audio band. The absolute input impedance level also is considerably lower for the current conveyors. This gives the multibit DAC optimum operating conditions. Novel scaleable architectures that offer easy current level optimization to any multibit D/A converter have been presented in this paper.

Some of the examined I/V converter circuits based on opamps exhibit surprisingly mediocre performance that does not justify their current reputation in some parts of the audio community.

Together with software calibration methods such as described in [4], the in this paper presented current conveyor circuits should enable a new level of performance in high-end D/A conversion equipment.

References

[1] D.C. Wadsworth: *"A Professional Audio Integrated Circuit"*, Preprint 2831, 87th AES Convention, New York, October 1989.

[2] C. Toumazou, F.J. Lidgey & D.G. Haigh: *"Analogue IC design: the current-mode approach"*, IEE Circuits and Systems series 2, 1990.

[3] Fred J. Highton & Toshio Murota: *"20 bit Colinear DAC, a Solution to Low Level Problems"*, Preprint 2963, 89th AES Convention, Los Angeles, September 1990.

[4] Niels O. Knudsen & Alain Moriat: *"A New Method for Linearization of a Classical-Type D/A Converter"*, Preprint 3966, 98th AES Convention, Paris, February 1995.

[5] Walt Jung: *"High Performance Audio Stages Using Transimpedance Amplifiers"*, The Audio Amateur, 2/92.

	Z_{in} @ 10Hz	Z_{in} @ 20kHz	Z_{in} @ 1MHz	Z_{in} @ 10MHz	Z_{in} @ 100MHz	f_{3dB} (MHz)
Voltage feedback opamp	4.0 mΩ	1.0 Ω	52 Ω	640 Ω	345Ω	38
Integrating voltage feedback opamp	4.0 mΩ	970 mΩ	2.7 Ω	8.2 Ω	36 Ω	(*)
Current feedback opamp	9.5 mΩ	12 mΩ	348 mΩ	3.5 Ω	40 Ω	71
Integrating current feedback opamp	682 mΩ	786 mΩ	1.3 Ω	2.9 Ω	17 Ω	(*)
Current conveyor	2.5 Ω	2.5 Ω	2.5 Ω	3.1 Ω	21 Ω	9.6**
Current conveyor with complementary compound input stage	112 mΩ	112 mΩ	115 mΩ	395 mΩ	21 Ω	9.5**
Current conveyor with active biased complementary compound input stage	7.0 mΩ	7.0 mΩ	26 mΩ	321 mΩ	21 Ω	9.4**
Current conveyor with active biased complementary compound input and output stages	6.7 mΩ	6.7 mΩ	25 mΩ	312 mΩ	21 Ω	10.2**

Table 1: Comparison between the different I/V converters.

Notes:
* This specification makes no sense in this case since the cut-off frequency of the integrating I/V converters is determined by an RC time constant.
** The cut-off frequency of the current conveyors is limited by an output capacitor.

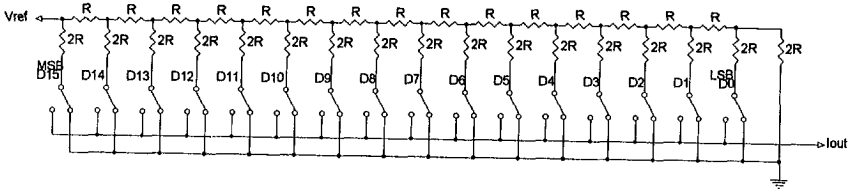

Fig. 1: 16 bit R-2R ladder DAC topology.

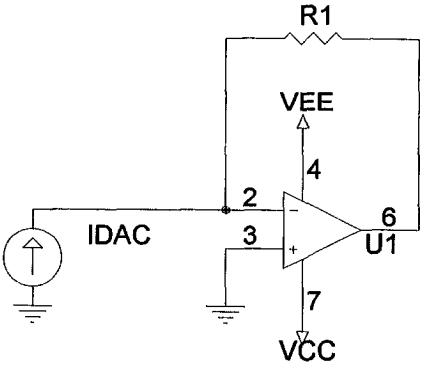

Fig. 2: I/V converter using a voltage feedback opamp.

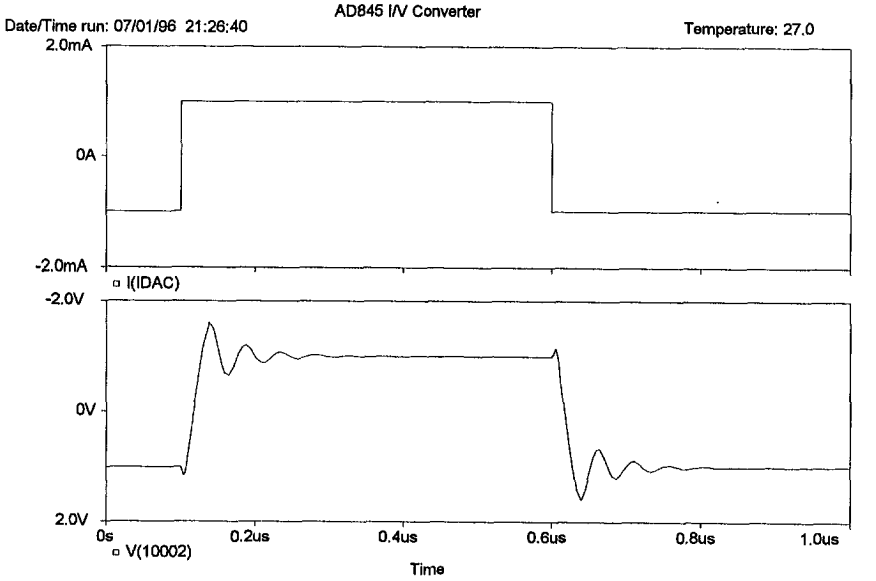

Fig. 3: Top: Input current
Bottom: Transient response of the circuit in fig. 2.

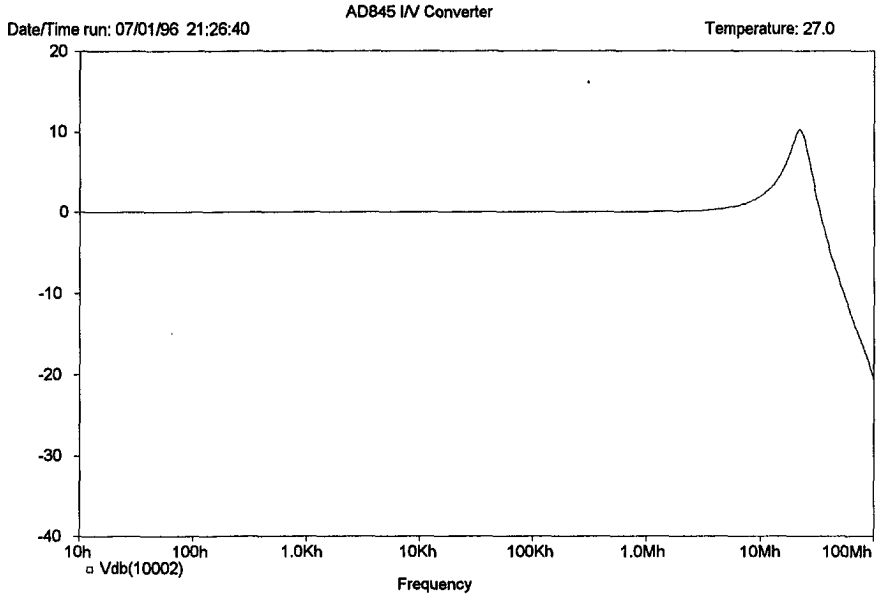

Fig. 4: Frequency response of the circuit in fig. 2.

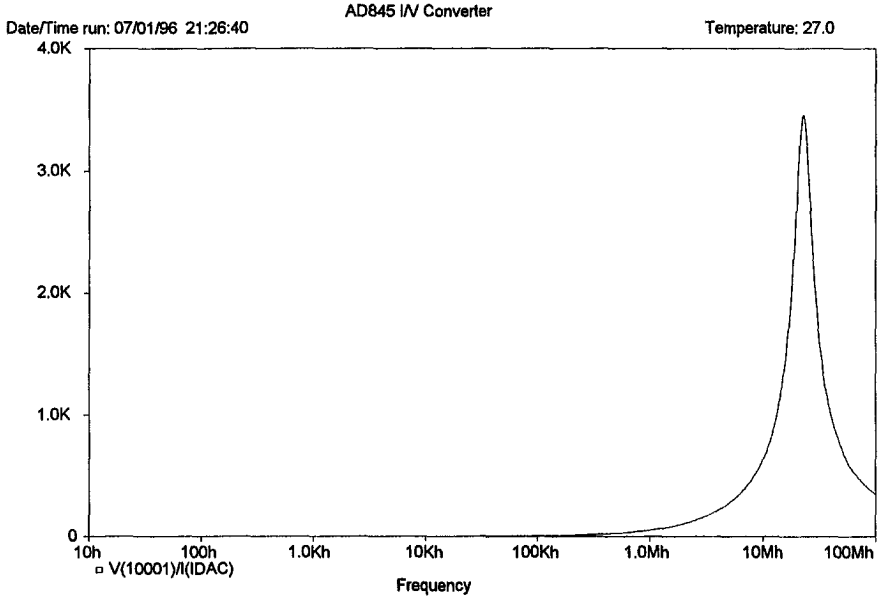

Fig. 5: Input impedance from 10Hz to 100MHz of the circuit in fig. 2.

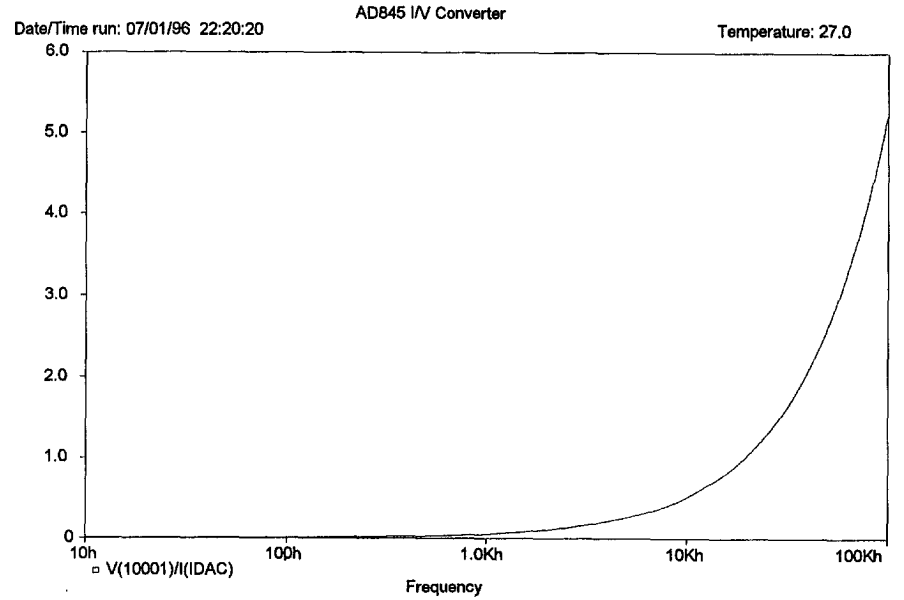

Fig. 6: Input impedance from 10Hz to 100kHz of the circuit in fig. 2.

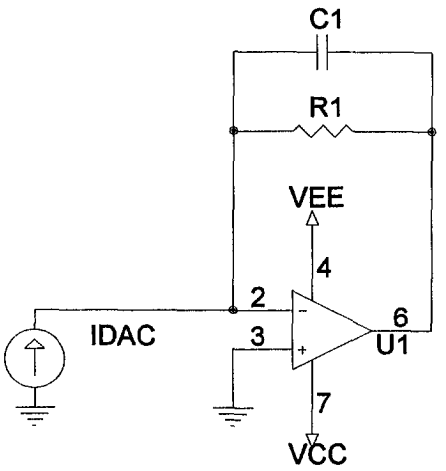

Fig. 7: Integrating I/V converter using a voltage feedback opamp.

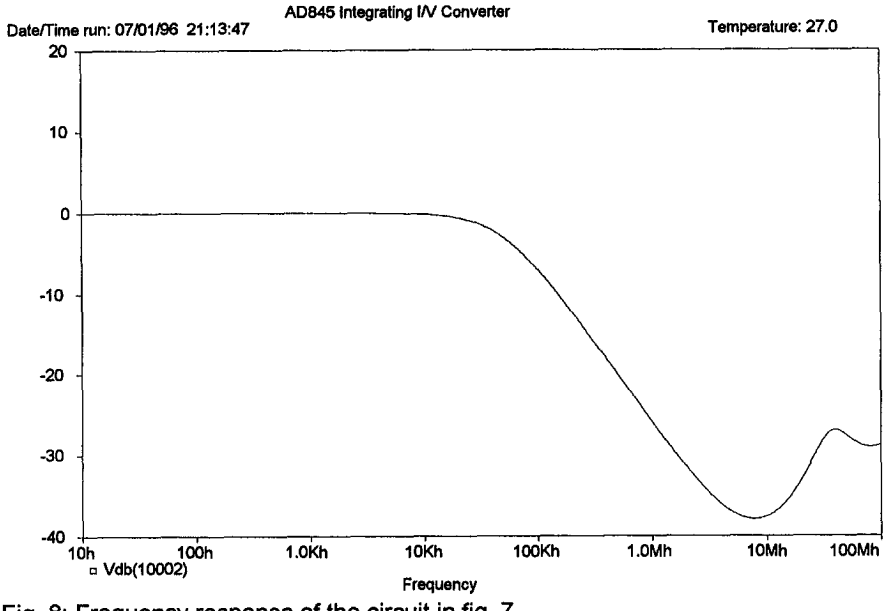

Fig. 8: Frequency response of the circuit in fig. 7.

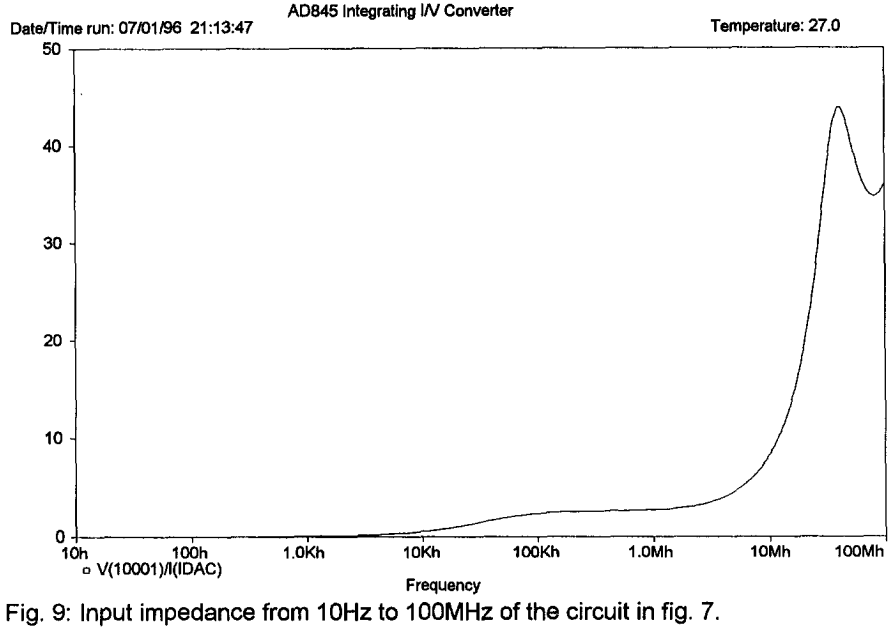

Fig. 9: Input impedance from 10Hz to 100MHz of the circuit in fig. 7.

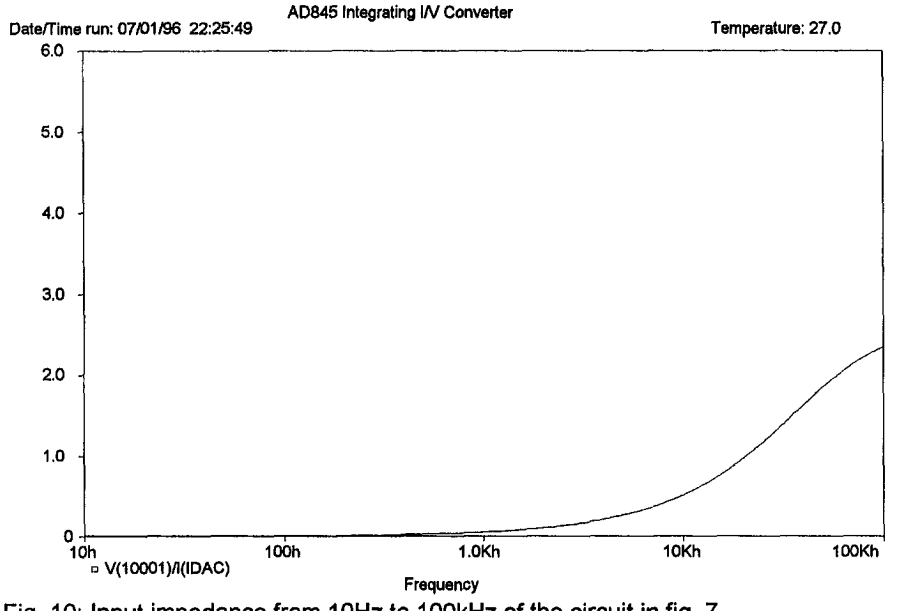

Fig. 10: Input impedance from 10Hz to 100kHz of the circuit in fig. 7.

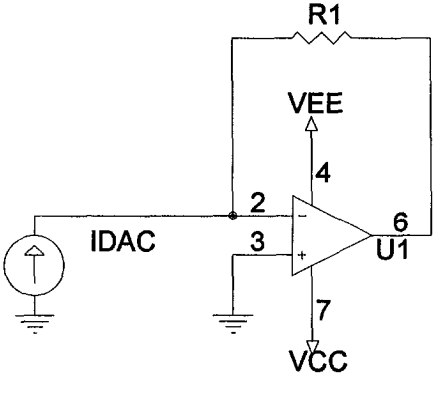

Fig. 11: I/V converter using a current feedback opamp.

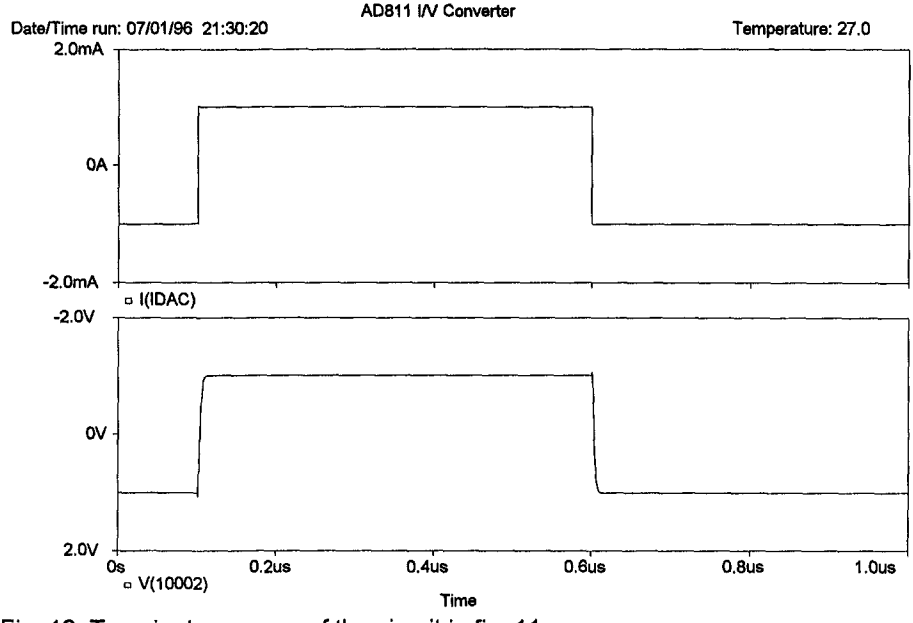

Fig. 12: Transient response of the circuit in fig. 11.

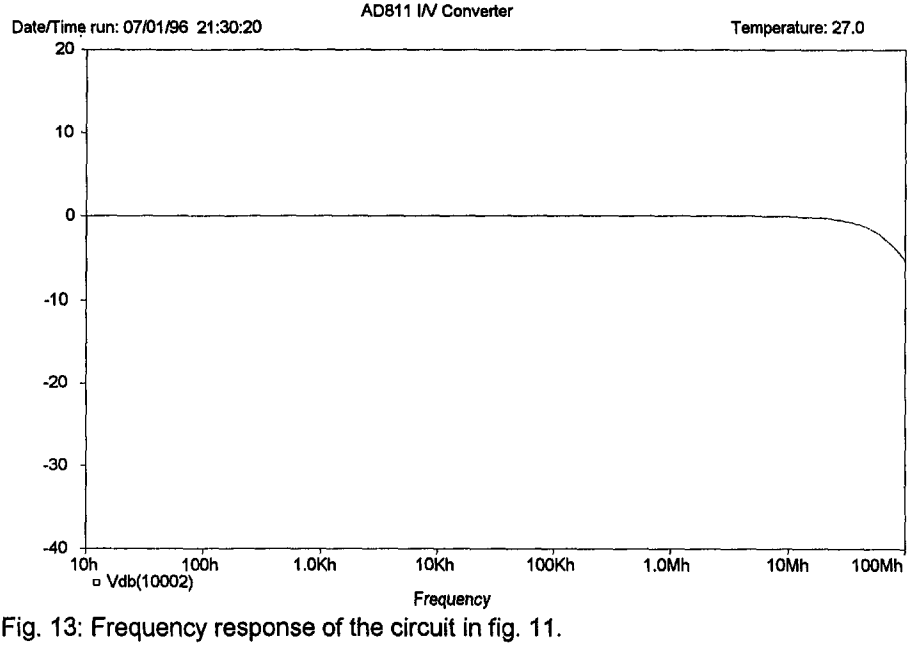

Fig. 13: Frequency response of the circuit in fig. 11.

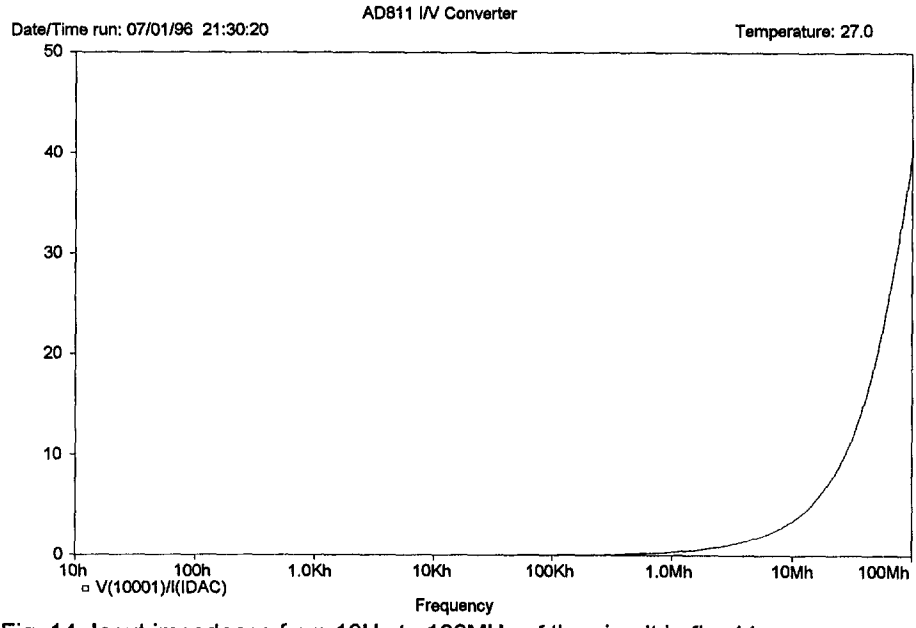

Fig. 14: Input impedance from 10Hz to 100MHz of the circuit in fig. 11.

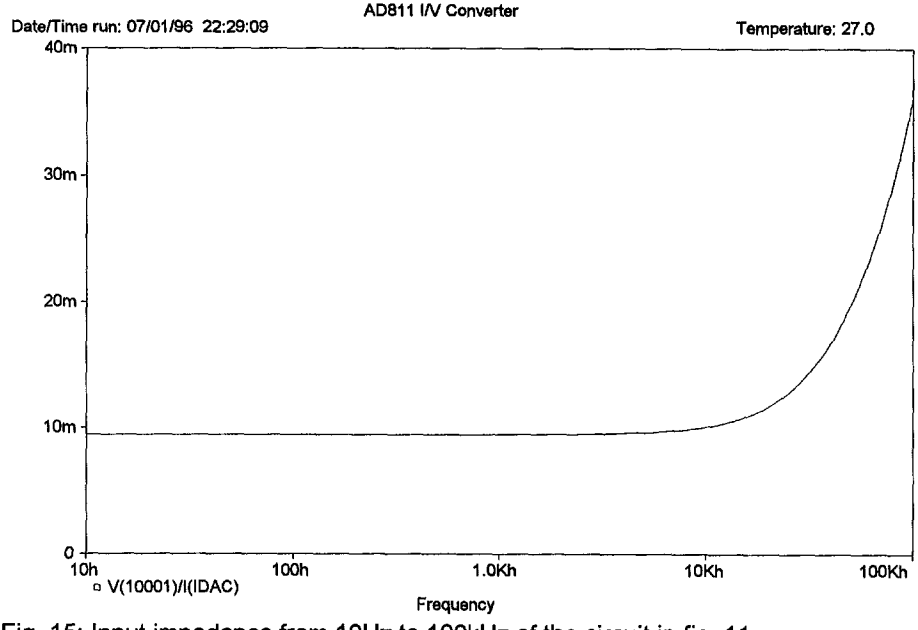

Fig. 15: Input impedance from 10Hz to 100kHz of the circuit in fig. 11.

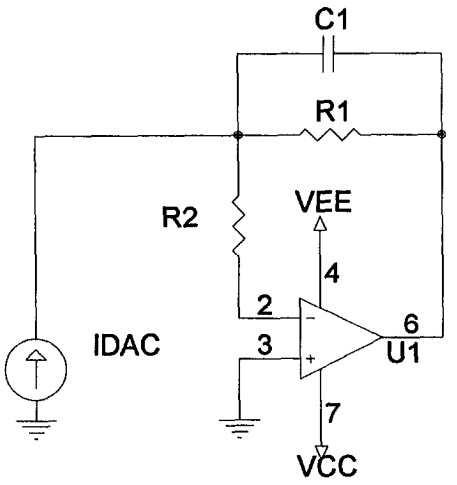

Fig. 16: Integrating I/V converter using a current feedback opamp.

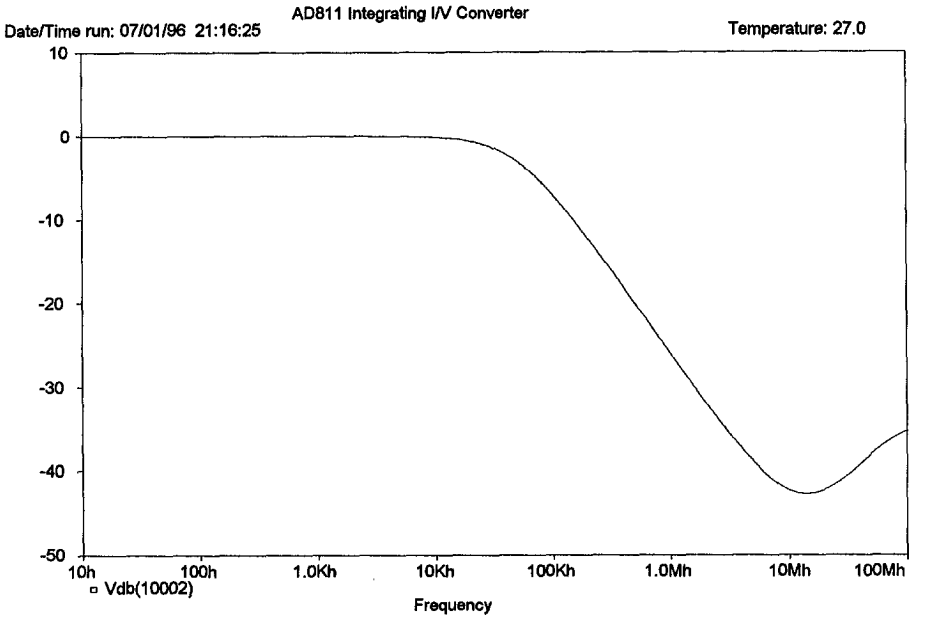

Fig. 17: Frequency response of the circuit in fig. 16.

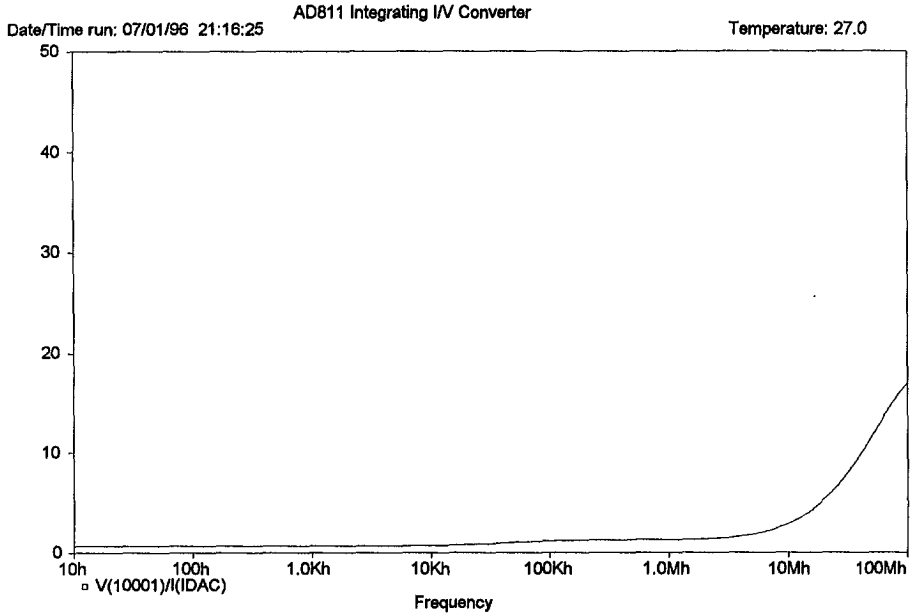

Fig. 18: Input impedance from 10Hz to 100MHz of the circuit in fig. 16.

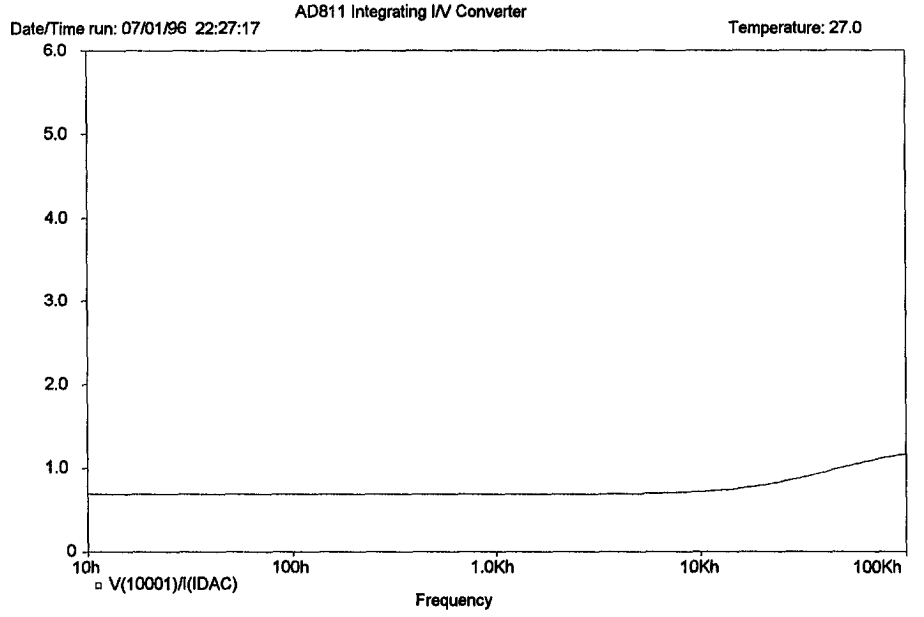

Fig. 19: Input impedance from 10Hz to 100kHz of the circuit in fig. 16.

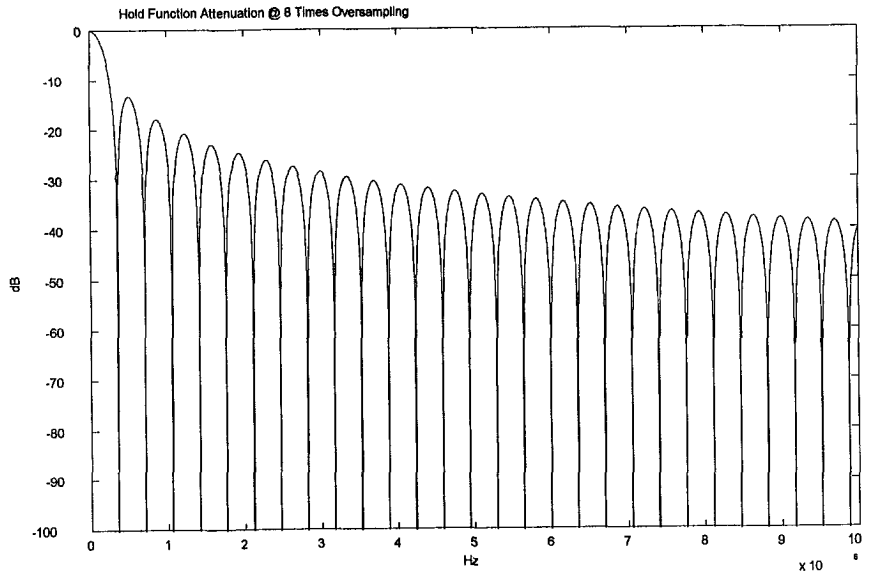

Fig. 20: Hold function attenuation from DC to 10MHz.

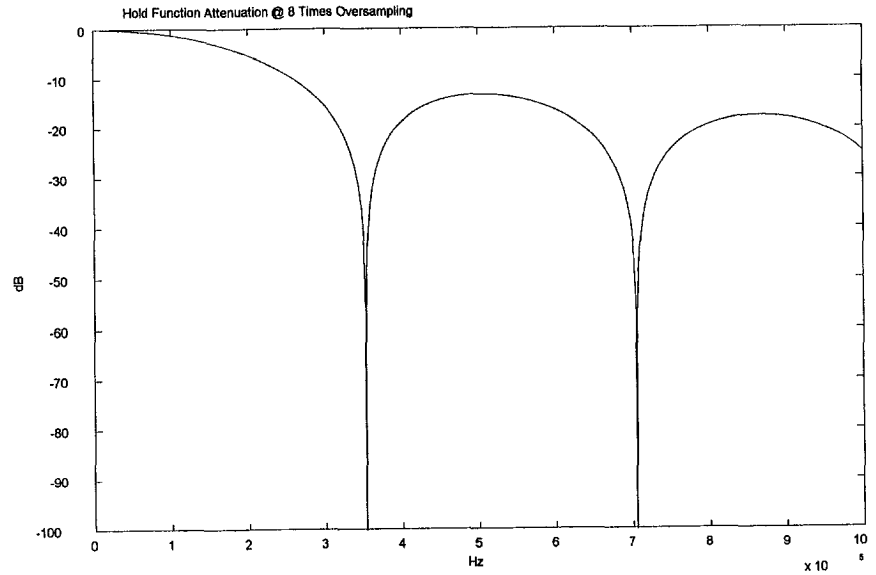

Fig. 21: Hold function attenuation from DC to 1MHz.

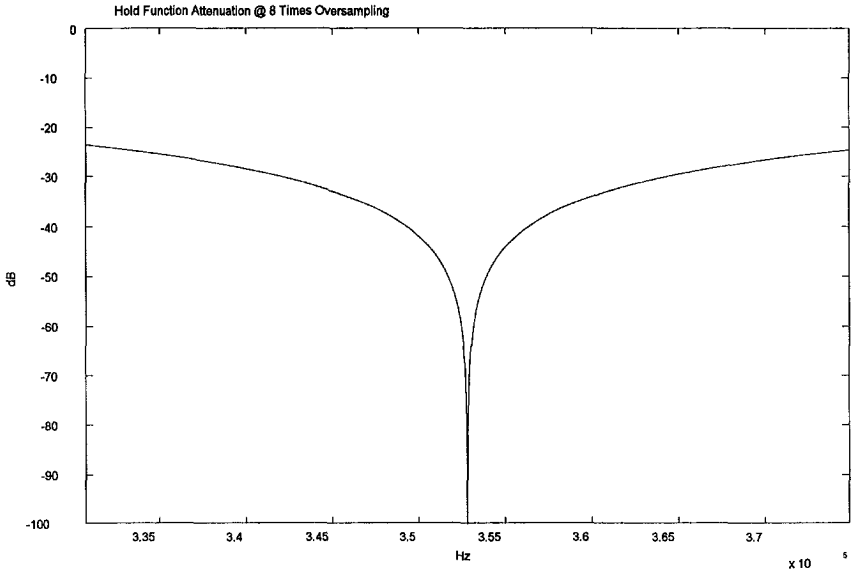

Fig. 22: Hold function attenuation at 352.8kHz ± 22.05kHz.

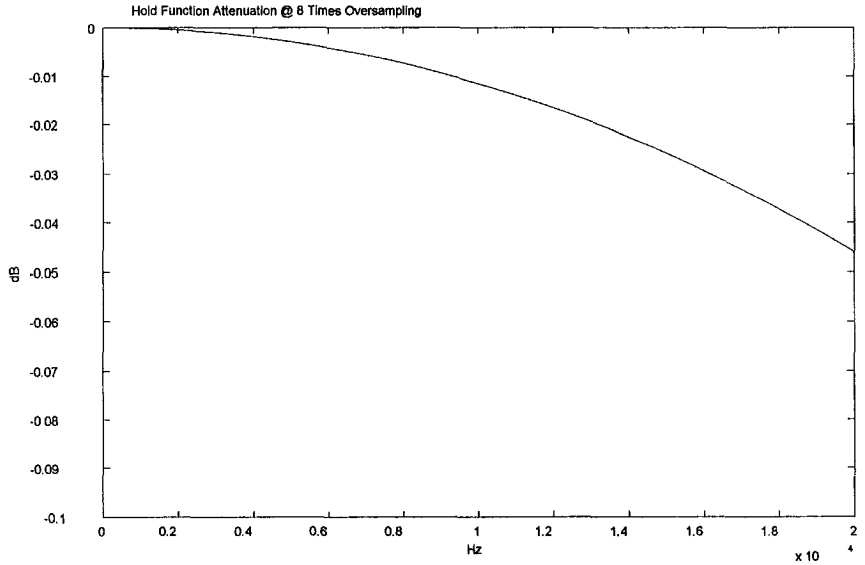

Fig. 23: Hold function attenuation from DC to 20kHz.

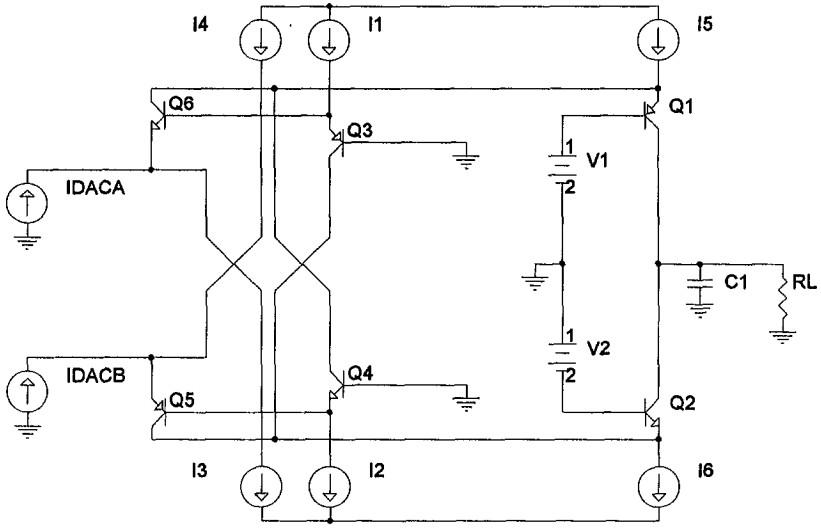

Fig. 24: Current conveyor.

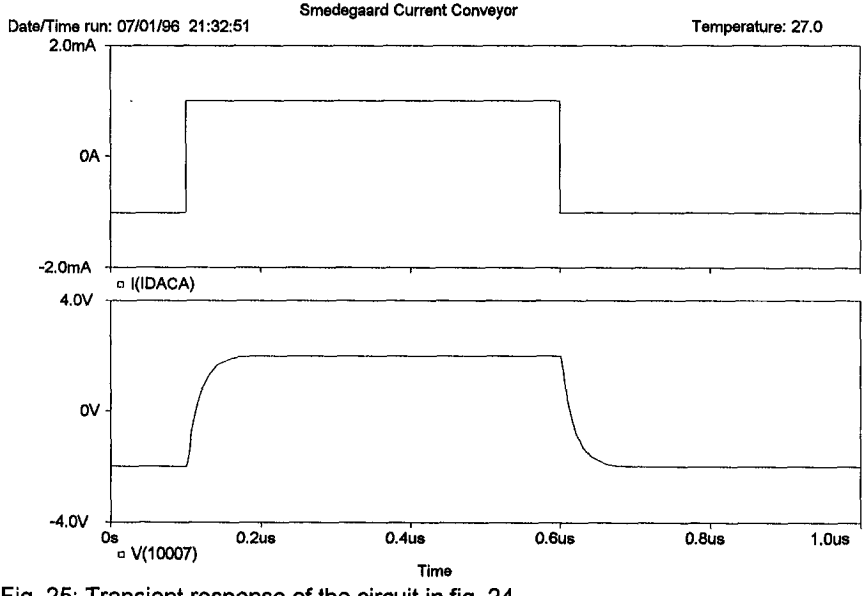

Fig. 25: Transient response of the circuit in fig. 24.

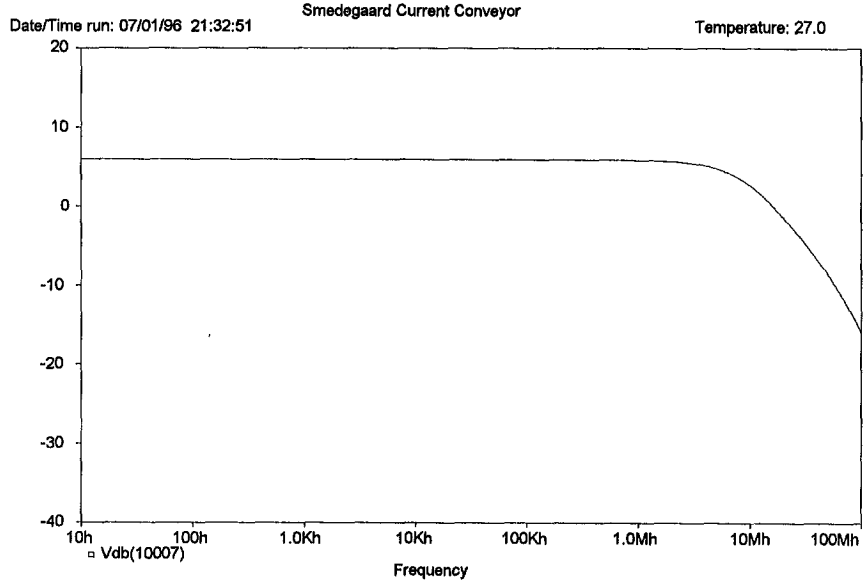

Fig. 26: Frequency response of the circuit in fig. 24.

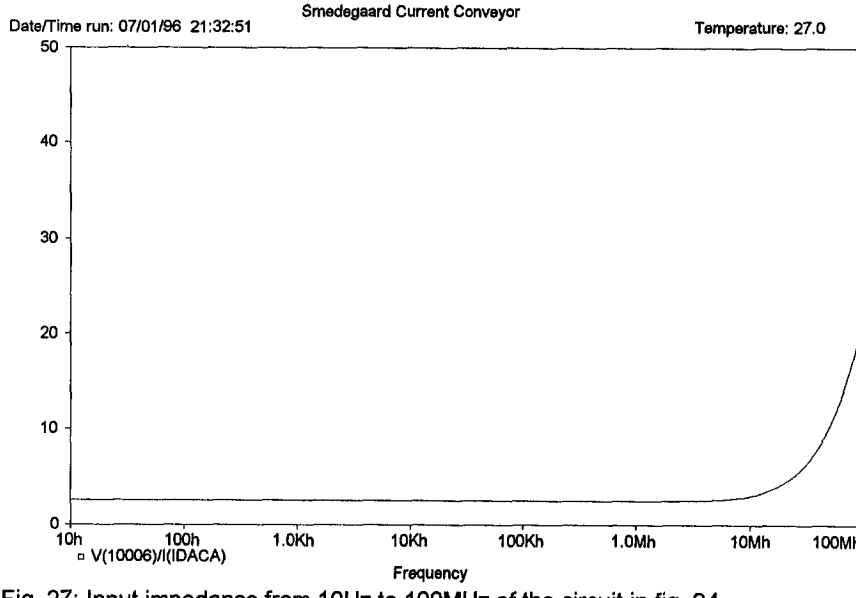

Fig. 27: Input impedance from 10Hz to 100MHz of the circuit in fig. 24.

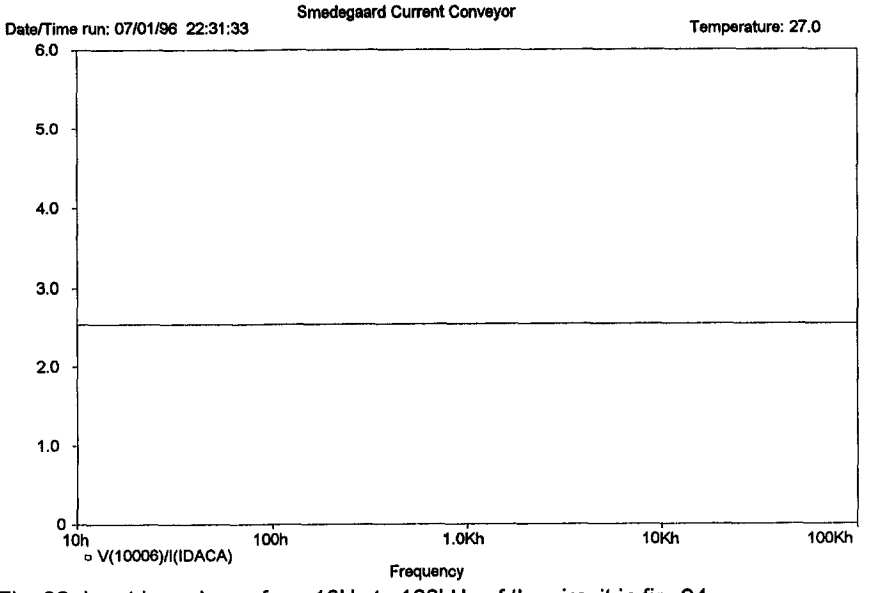

Fig. 28: Input impedance from 10Hz to 100kHz of the circuit in fig. 24.

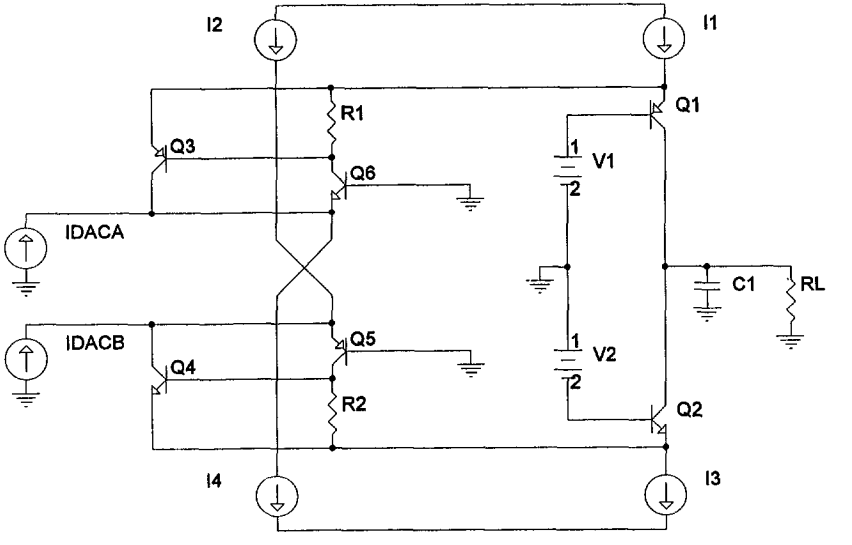

Fig. 29: Current conveyor with complementary compound input stage.

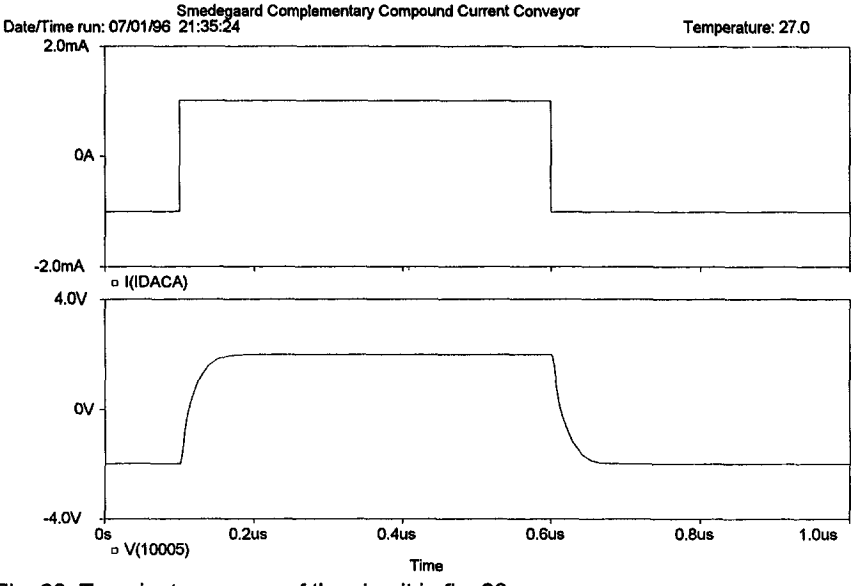

Fig. 30: Transient response of the circuit in fig. 29.

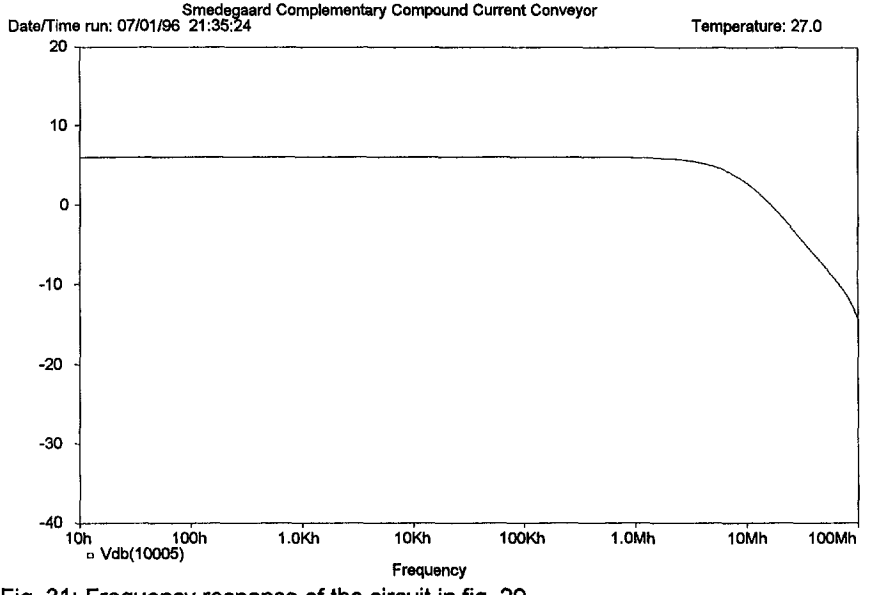

Fig. 31: Frequency response of the circuit in fig. 29.

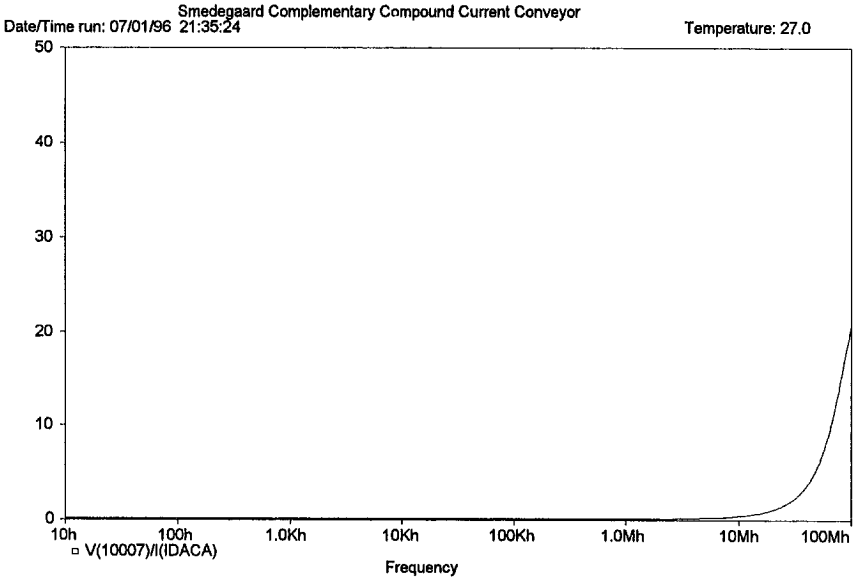

Fig. 32: Input impedance from 10Hz to 100MHz of the circuit in fig. 29.

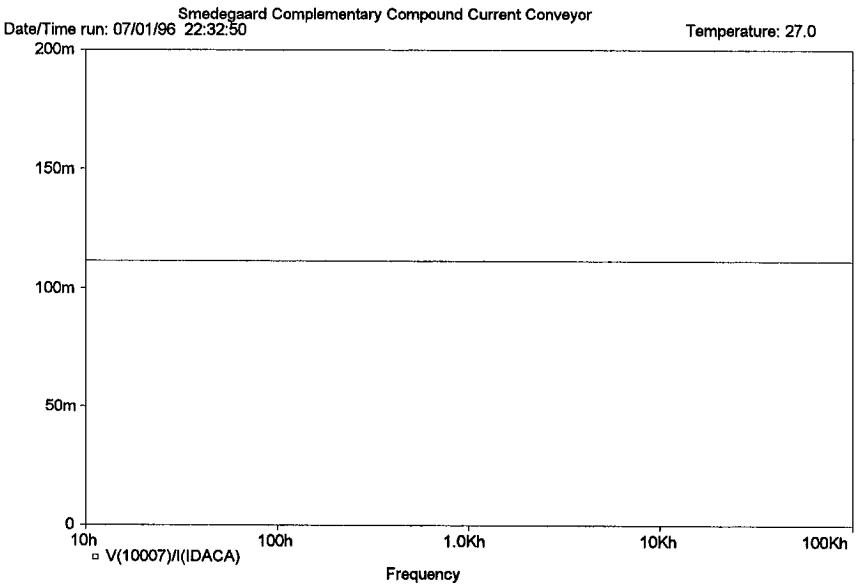

Fig. 33: Input impedance from 10Hz to 100kHz of the circuit in fig. 29.

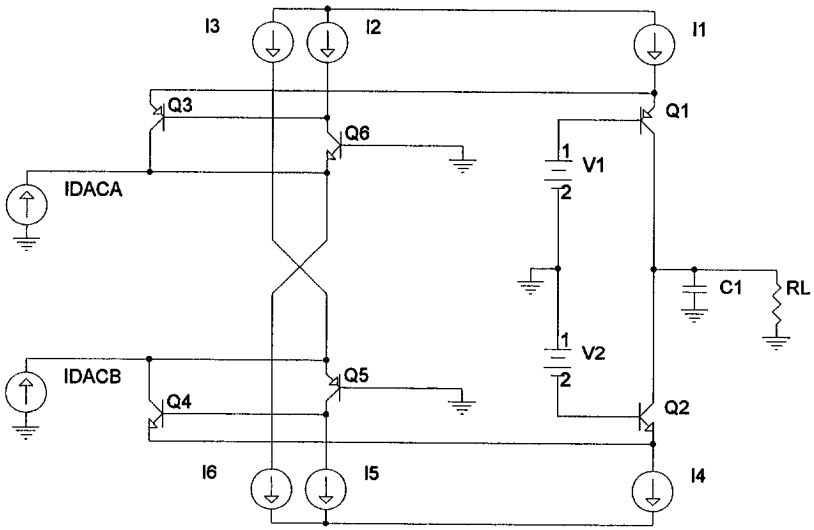

Fig. 34: Current conveyor with active biased complementary compound input stage.

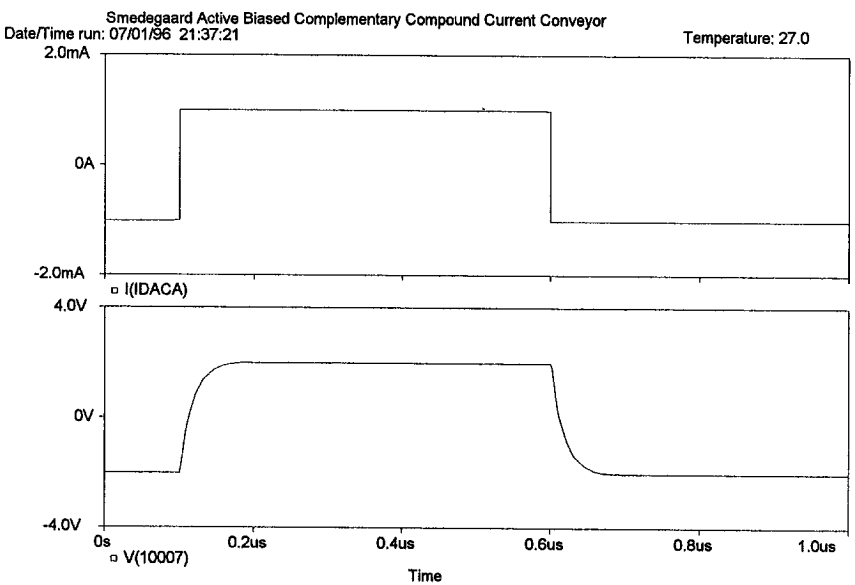

Fig. 35: Transient response of the circuit in fig. 34.

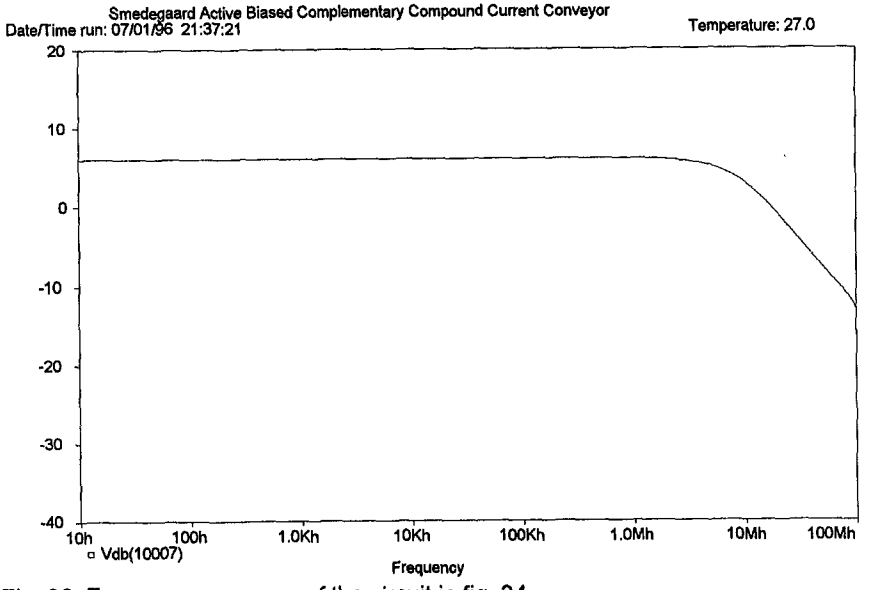

Fig. 36: Frequency response of the circuit in fig. 34.

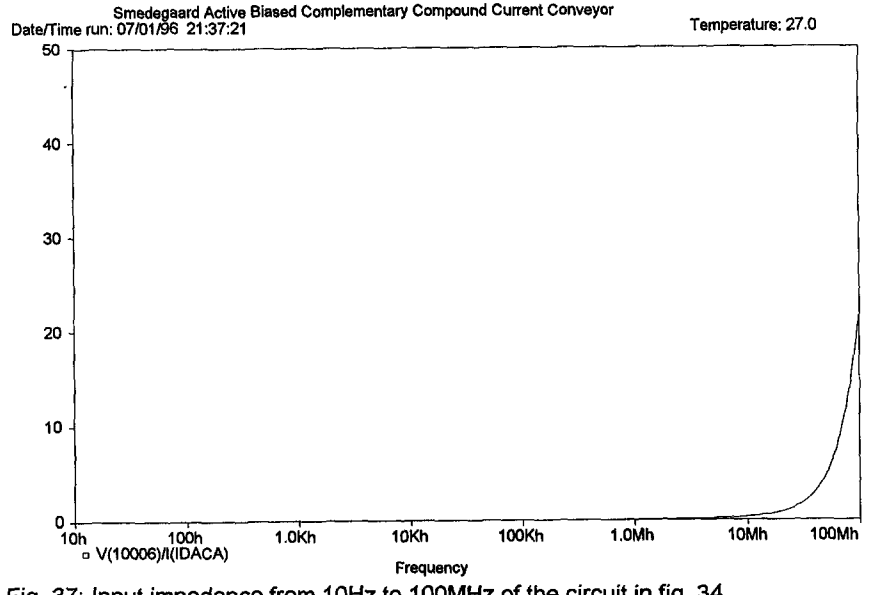

Fig. 37: Input impedance from 10Hz to 100MHz of the circuit in fig. 34.

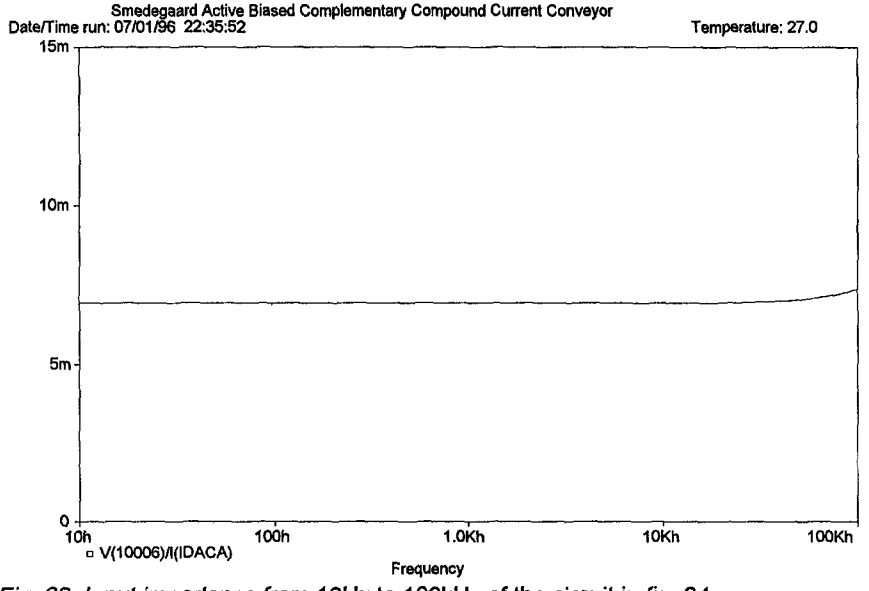

Fig. 38: Input impedance from 10Hz to 100kHz of the circuit in fig. 34.

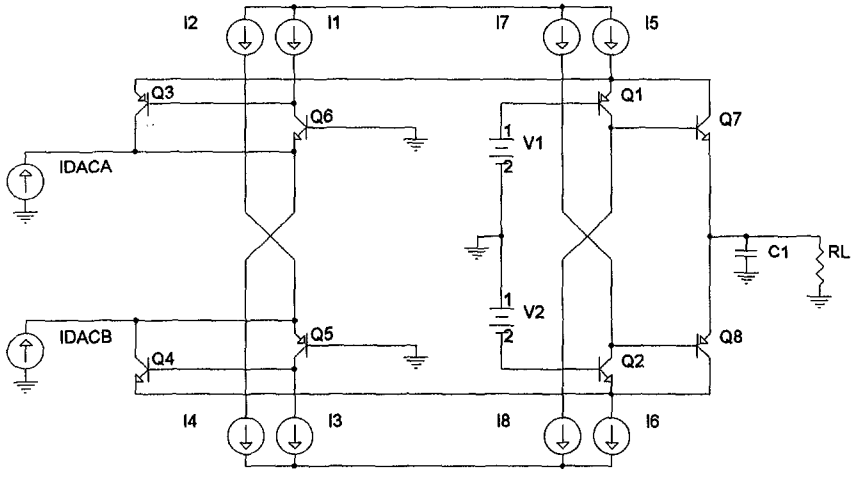

Fig. 39: Current conveyor with active biased complementary compound input and output stages.

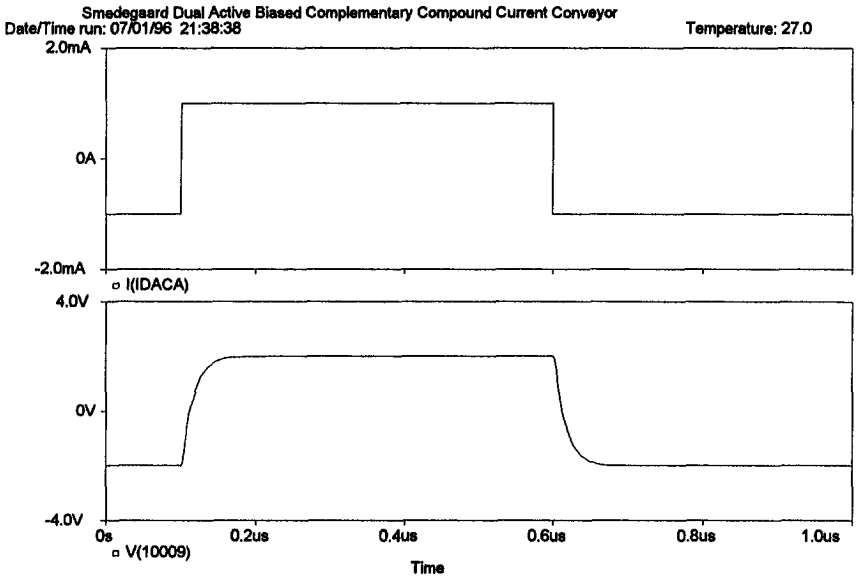

Fig. 40: Transient response of the circuit in fig. 39.

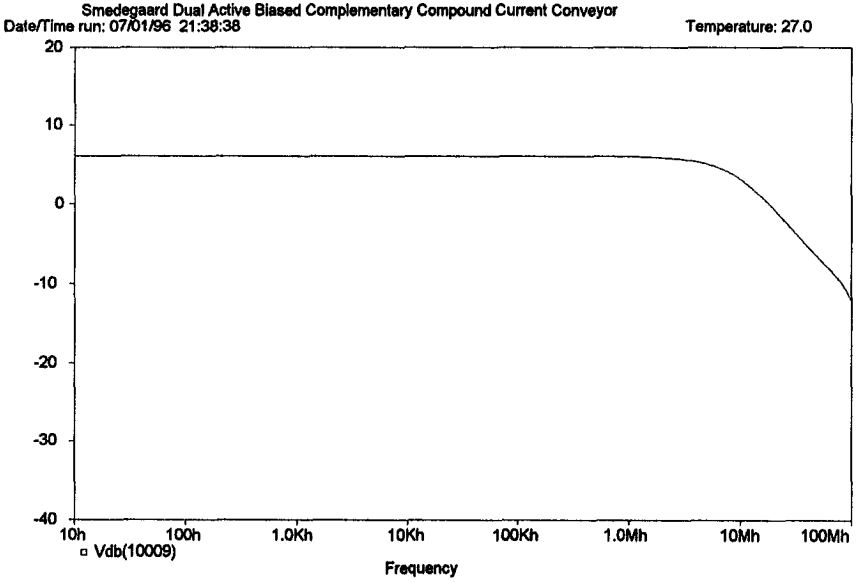

Fig. 41: Frequency response of the circuit in fig. 39.

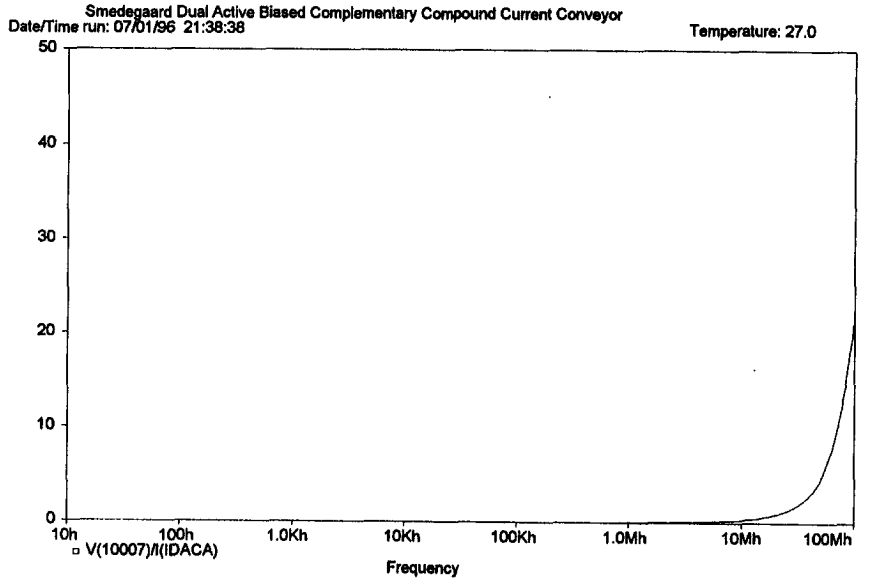

Fig. 42: Input impedance from 10Hz to 100MHz of the circuit in fig. 39.

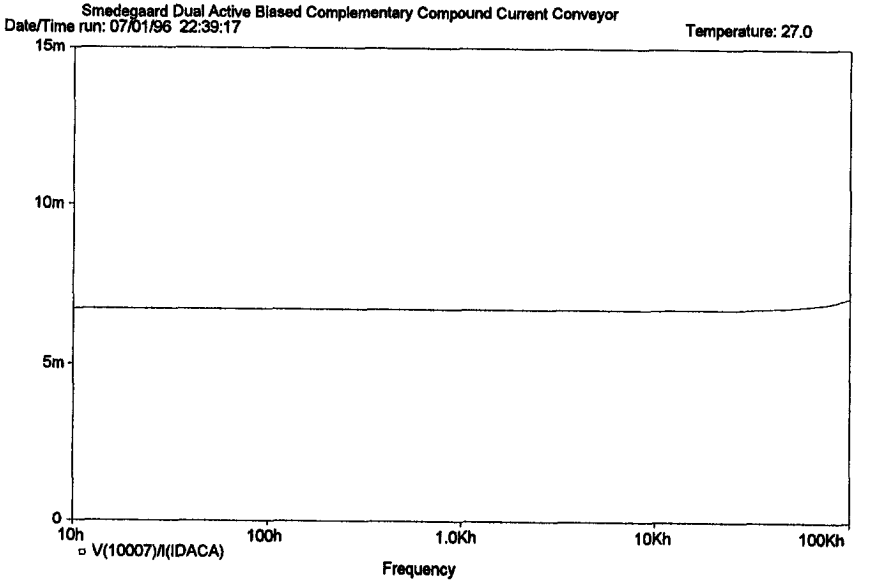

Fig. 43: Input impedance from 10Hz to 100kHz of the circuit in fig. 39.