



H_{fe} and V_{be} matching is not necessary in my circuit because the current sources are adjustable. They also compensate for I_{DSS} differences in the FETs. I found that the P channel variety has lower I_{DSS} usually and matching them is time consuming and not funny at all. You have literally to buy hundreds to have some success because FETs have much higher spread of parameters than BJTs do. In my design you can simply use the FETs and the BJTs straight out of the tube or any other package they come in. The parallel symmetric design has also the advantage of distortion cancelation of second harmonic, the major source of distortion in a single ended FET – BJT cascode. Third harmonic is low in a FET – BJT cascode anyway.

So we have a fast, low noise, low distortion balanced input stage. It's time to discuss the rest. First let's look at the circuit diagrams (Figs 10a and 10b). A detail that I have not discussed when explaining the input stage is the unusual biasing of the cascode transistors. It is simply a resistive divider fed by the constant current sources. This arrangement is called ground referenced common base stage.

It is a rare sight and I first spotted it in a design by Hugh Dean of AKSA fame. It has several advantages: simplicity, low noise because a separate bias source with potential noise is not necessary and a measure of current feedback that stabilizes the gain, lowers distortion and raises the bandwidth a bit at the cost of less gain.