Letter to the Editor

Dear Editor,

In his Letter to the Editor, commenting on Stuart Yaniger's Cathodyne article in Linear Audio Volume 0, Burkhard Vogel has presented an excellent analysis, and I agree with just about everything that he has to say. In fact, I had derived his equations (1) – (3) myself some time ago for my own benefit.

As long as we recognize that there are some cases in which the plate and cathode loads will not be identical during normal Cathodyne use, there is nothing wrong with analyzing Cathodyne operation as if it were a "floating" driver (of approximate impedance 2/gm) driving a single floating load instead of the two single-ended identical loads that it actually does. None of this has ever been in contention. Neither my nor Peter van Willenswaard's analysis ever even addressed this point of view of the circuit, let alone disagreed with it.

From a different point of view, Mr. Vogel has explicitly recognized that the Cathodyne must confront some unbalanced situations such as those associated with PSRR and CMRR. I would like to add to those the important case of when one of the two power tubes draws grid current and unbalances the loads. To address this, Mr. Vogel has thoughtfully provided on page 8 of his MathCad analysis a Section 2.2 entitled "Output resistances (between respective output and ground!)." His expressions for the plate ($R_{o.a}$) and cathode ($R_{o.c}$) impedances show that the former is indeed much larger than the latter, replicating my results (equations 18 and 19 in my letter) and confirming what Mr. van Willenswaard said in his letter.[1] This difference in cathode to ground and plate to ground impedances is important. To verify this, all you need to do is to bench test or simulate the difference in the power tube grid signals when the Cathodyne cathode draws grid current, and when the plate does.

With all this said, I admit to being a bit surprised that Mr. Vogel says, "Stuart is absolutely right…" I count a number of significant disagreements between the two.

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[1] It's easy to show that these results also apply to both real-world "balanced" (1) and ideal (2) Cathodynes:

1. No physical Cathodyne is perfectly balanced – all have some imbalance due to component tolerances. The imbalance can be thought of as an extra load resistor on the plate or cathode, an "unbalanced" situation to which these equations apply. This small imbalance in no way detracts from the balanced driver analysis in Mr. Vogel's equations (1) – (3), however, which is still essentially valid.

2. Perform an algebraic analysis of the idealized, perfectly balanced Cathodyne. Connect equal and opposite ground-referenced AC current sources ip and ik to the plate and cathode respectively of a Cathodyne with no grid excitation. This Cathodyne is balanced. Derive expressions for the plate and cathode voltages Vp and Vk in terms of ip and ik. Each current will make a contribution to each voltage. Now recall that the impedance between nodes A and B equals the change in voltage between A and B due to a current flowing from A to B, divided by that current. So to get the plate to ground impedance, we must divide only that portion of Vp which is due to ip, since only ip flows directly from plate to ground. (The same sort of thing is true for the cathode.) The results are the same as Mr. Vogel's $R_{o.a}$ and $R_{o.c.}$

Mr. Vogel consistently refers to $R_{o.bal}$ and draws one floating differential driver in figures 2, 3 and 4 with no ground references. He never once refers to the anode or cathode impedances in this situation, because the operant impedance for balanced situations is Zpk, the impedance *between* the plate and cathode, not those between one or the other output and ground.

Mr. Yaniger, however, repeatedly refers in the balanced situation to a plate impedance that is identical to a cathode impedance. Now, when one says "input impedance" or "output impedance", it is generally understood that this means the impedances between input and ground, or output and ground respectively. No impedance is associated with a single node only. With no other possible physical node to use as a reference, Mr. Yaniger must be doing the same. If so, then Mr. Yaniger's claim of equal impedances directly contradicts Mr. Vogel's section 2.2 equations showing that they are different.

Next, refer to Mr. Yaniger's Figure 3 circuit showing the plate and cathode in two separate circuits, united by a "common" node that doesn't physically exist. He instructs us that in order to measure the short circuit current, "BOTH nodes need to be shorted…," presumably to ground (because the common node doesn't exist) and not simply to each other, because "BOTH nodes need to be shorted to each other" is a Department of Redundancy Department redundancy. But if this is meant to be understood as a floating two-node driver, the proper procedure to determine a standard two-node Thevenin equivalent involves shorting just the plate and cathode together, not to each other *and* ground, to determine the short circuit current. There are no separate plate and cathode drivers with equal impedances of 1/gm; there is a single plate-to-cathode driver with an approximate impedance of 2/gm.

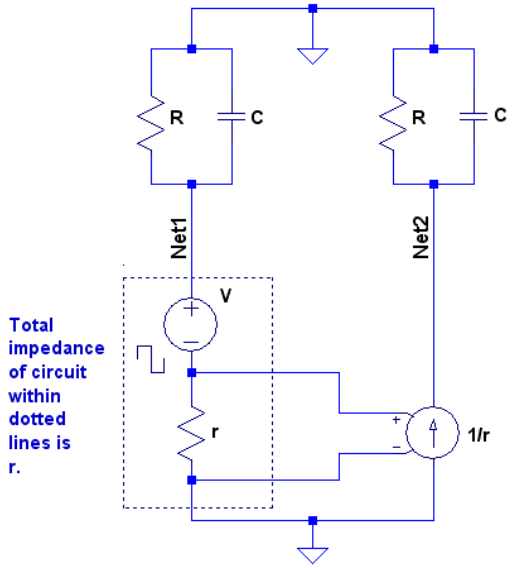
Finally, we come to the Rise Time test in which it is again asserted that "the effective source impedance at each terminal is equal." The logic here seems to be something like

Claim: only equal source impedances can lead to equal rise times across equal loads.

Observation: The rise times and loads are equal.

Conclusion: The source impedances are equal.

The problem here is with the claim. The following simple circuit shows that it is not generally true:



A square wave voltage V source drives a parallel R-C network of impedance Z terminated by the input of a unity-gain current mirror. The mirror has an input impedance of r and a transconductance of 1/r. The mirror drives a second network of impedance Z identical

to the first. Identical currents flow through the networks, so the voltages across them are identical, as therefore must be the rise times. But the drive impedances of the two networks are about as different as can be: r for the first network, and infinity (ideal current source) for the second.

We see that identical rise times across identical networks do not imply identical driving impedances. The Cathodyne rise time test does not imply equal drive impedances.

Throughout his article, Mr. Yaniger seems to conceptualize the balanced Cathodyne as having two back-to-back (ground-referenced?) sources of identical impedances. Such, if it were true, would lead to a massive discontinuity in plate and cathode impedances as the loads changed from perfect balance (1/gm = 1/gm) to even a 0.001% imbalance ($R_{o.a} >> R_{o.c}$.)

Mr. Vogel, on the other hand, correctly and clearly sees a single two-node floating differential driver with a single impedance in the balanced case. He also recognizes that the plate to ground impedance is much higher than that of the cathode to ground, even given the validity of the balanced driver viewpoint. There is nothing inconsistent with these two views.

I'm with Mr. Vogel's presentation on this one. I'd be very interested to hear his thoughts on the differences I mentioned above.

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