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Notch filter autotunes for audio applications

John R Ambrose, Mixed Signal Integration, San Jose, CA

Tracking notch filters find use in harmonic-distortion analyzers; they also can remove heterodyne noise from ham-radio systems. A conventional tracking switched-capacitor notch filter relies on a bandpass filter, a voltage-to-frequency converter, and a notch filter to track the incoming signal and remove undesired tones. The bandpass filter in these circuits sometimes adjusts to the wrong frequency, meaning that the undesired tone would have no attenuation.

The circuit in this Design Idea uses IC_1 , a 74HC4046 PLL (phase-locked-loop) IC, which operates as fast as 1 MHz, to improve the noise immunity of the system (**Figure 1**). IC₂, an RDD104 IC from LSI Computer Systems Inc (www.lsicsi. com), provides a 1000-to-1 divider in an eight-pin package. IC₃, Mixed Signal Integration's (www.mix-sig.com) MSHN5 1000-to-1 clock-to-corner switched-capacitor highpass/notch filter, comes in an eight-pin package.

You feed IC_1 's VCO (voltage-controlled oscillator) output into the clock input of IC_2 . IC_2 can perform 10-, 100-, 1000-, and 10,000-to-1 divisions using the DIV1 and DIV2 pins. You tie the output of RDD104 to the COIN of IC_1 . By using IC_1 's EX/OR phase comparator, you

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can improve noise immunity. You apply the input signal to both IC_1 and the input of IC_3 , whose clock you derive from the CLKOUT pin of IC_2 .

CLKOUT pin of IC₂. The MSHN5, IC₃, contains both selectable highpass filters and selectable



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Figure 2 You feed the circuit an input tone (top trace) and get the output signal from the MSHN5 (second trace). The third and fourth traces represent the clock signal from the 74HC4046 PLL. notch filters. When you tie the FSEL pin high, it selects notch; tying TYPE to AGND selects the narrow notch filter. This step ensures the removal of only one tone from the input signal with little information loss. IC₃'s 1000-to-1 clock-to-corner ratio reduces the chance that aliasing signals will affect the output. For voice applications, for example, no signals of 500 kHz or higher would be available to alias into the passband. A sample setup uses an input frequency of 789.13 Hz at a clock frequency of 789.13 kHz, 1000 times the input signal (**Figure 2**). The PLL tracks the input, moving the notch filter to 1.24 kHz.EDN

Image-capture system uses USB and LabView

Chien-Hung Chen and Po-Jui Chen, National Applied Research Laboratories, Hsinchu, Taiwan

Capturing and processing graphical images requires manipulating data into a form that you can use. This Design Idea describes an imaging system using a USB (Universal Serial Bus) image-capturing system that uses OmniVision's (www.ovt.com) 640×480-pixel, 8-bit-color OV7660 image sensor. The CY7C68013A-128AXC from Cypress Semiconductor (www.cypress.com) provides a USB interface between a PC and the image sensor (**Figure 1**). The control software is written in LabView from National Instruments (www.ni.com/ labview).

To avoid losing data from the image sensor, the system employs a data buffer in the image-processing algorithm. The buffer uses system memory for data storage. The queue ensures that the system will not lose data regardless of how much time it takes to process each row in an image. This technique is useful in measurement systems in which the speed of data acquisition and data processing may differ.

Figure 2 shows the programming flow chart. After the system starts, you must set the driver to NI-VISA (Virtual Instru-

ment Software Architecture), a software layer that provides a common programming interface across many types of measurement instruments and software drivers. Once you set the driver, you can initiate the USB device. LabView provides a driver wizard that helps you to build drivers. The LabView code for this graphicsystem design can easily implant USB data transmission and its applications. You can download the LabView code from the online version of this Design Idea at www.edn.com/100624dia.

After initializing the USB device, the software allocates system memory in a FIFO (first-in/first out) configuration to become the data buffer. A memory endpoint sets the input buffer's size to 4 kbytes. The software then reads the image in rows and stores data from the sensor in the buffer memory. After reading the data from the buffer, the system image uses two threads to process the data.

Figure 3, available with the online version of this Design Idea at www.edn. com/100624dia, shows the LabView programming diagram for USB data transmission. The program includes for-loop pro-



cedures for storing the image in the buffer memory, reading and processing image data, and performing state checking.



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The main processing algorithm obtains and displays red, green, and blue data of each pixel. **Figure 4**, available with the online version of this Design Idea at www.edn.com/100624dia, shows the test result. The element in the buffer shows that the system processed 614,400 pixels. The actual amount will vary based on the PC's performance. A powerful PC can smoothly run this program, whereas a weak PC will cause the data to accumulate in the buffer.EDN

Low-cost RF synthesizer uses generic ICs

James B Wood, Inovonics Inc, Felton, CA

You can design a hardware-based frequency synthesizer with one inexepensive IC and a few passive components. Such synthesizer chips are not always available, however, because they are typically single-sourced and are not in stock with parts distributors. The need for a working circuit in a short time and using common parts prompted the creation of the circuit in this Design Idea. The synthesizer covers the US commercial AM (amplitude-modulation) broadcast band. It tunes in 10-kHz steps from 500 to 1800 kHz, but you can scale the frequencies for other applications.

The PLL (phase-locked loop) time base is a 100-kHz, tuning-fork-cut crystal of the same size as those in wrist watches. Using a more common crystal requires some extra parts to scale the frequency. Note that if you attempt to use one of these tiny crystals with a CMOSgate oscillator circuit, however, the circuit will either fail to start or exhibit visible jitter. A discrete-transistor Franklin oscillator, such as the one comprising Q_3 and Q_4 works better (**Figure 1**). This circuit also works well in the VCO (voltage-controlled-oscillator) portion of the synthesizer.

You use IC_{4A} , one-half of a 74HC390 dual decade-divider IC, to divide the 100-kHz reference into the 10-kHz frequency that the PLL uses. This 10-kHz square wave feeds one input of the phase comparator, IC_3 , and drives a voltage-tripler circuit comprising D_{12} through D_{15} . This tripler creates approximately 12V and obviates the need for a second higher-voltage power rail. You need the 12V to bias the VCO's varactor diode to the top of its tuning range.

The VCO, comprising Q_1 and Q_2 , runs at twice the desired output frequency. Varactor diode D_1 and inductor L_1 provide a tunable tank circuit. Any varactor for AM-radio tuning should



work. The capacitance of these diodes varies from 500 pF with no dc bias to 25 pF with a 12V reverse bias. IC_{1A} divides the LC oscillator by two to yield a symmetrical output waveform.

 IC_2 further divides the VCO to the PLL's frequency. IC_2 , an eight-stage binary counter, resets itself to zero when it reaches the desired count. IC_{IB} , a pulse-stretching one-shot, ensures that all sections of IC_2 reset at the target count. You program the divider with DIP switch S_1 . Diodes D_2 through D_9 supply the necessary AND-logic function.

To set the synthesizer frequency, you first calculate the required divisor. For a 1140-kHz output, you must divide the VCO by 114 to equal the PLL's frequency of 10 kHz. You can close the DIP switches in S_1 —in this case, switches 64, 32, 16, and 2—so that the numbers add up to the divisor: 114.

The PLL comparator is a three-state phase and frequency detector (**Reference** 1, in the online version of this Design Idea at www.edn.com/100624dib). When the divided VCO frequency is greater than 10 kHz, the \overline{Q} output of IC_{3B} goes high and

the Q output of IC_{3A} pulses at a 10-kHz rate. This action turns on Q₆, back-biasing D₁₆ to create a high-impedance state with respect to the 12V supply. Loop-filter capacitor C₂ then discharges through R₁₅ and Q₅. When the divided VCO is lower than the loop frequency, the Q output of IC_{3A} goes low, turning off Q₅ and creating a high-impedance state with respect to ground. Q₆ now pulses on and off, allowing C₂ to charge through D₁₅ and R₁₆. At PLL lock, Q₅ is off and Q₆ is on, except for a narrow "keep-alive" pulse at the loop frequency.EDN

Tricolor LEDs create a flashing array

Jeff Tregre, www.BuildingUltimateModels.com, Dallas, TX

You can build a matrix of RGB (red/green/blue) LEDs using a simple and inexpensive circuit comprising the control logic and driver circuit in **Figure** 1 and some LEDs (**Figure 2**). The center RGB LED is the first to come on, after which each sequential LED in the 8×8-LED matrix follows. This process gives the appearance that the display is alive and moving outward. This sequence repeats, producing a rainbow effect of colors.

You can adjust the frequency of each clock by changing the values of R_{17} , R_{19} , and R_{23} . Use different frequencies for each clock, which will display eight colors from the 65 tricolored LEDs, because using the same frequencies for all the clocks causes your display to appear white. The cost of building this circuit

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should be \$25 to \$30. You can purchase 100 5-mm RGB LEDs from eBay for a total of about \$18. Be sure to use common-cathode LEDs.

This simple circuit comprises three clocks and three counters, one for each

of the three LED colors. Setting each clock frequency to a different rate causes each color of each LED to appear to be random. All resistors are 0.25W, except for R_3 , R_8 , and R_{13} , which are 0.5W; R_4 , R_9 , and R_{14} , which are 1W; and R_5 , R_{10} ,

and R_{15} , which are 1.5W resistors. These high-wattage resistors and the 12 NPN transistors are necessary because all LEDs in this matrix, except the center one, connect in parallel. Start by bending all of the ground leads flat and connecting



them together. When wiring the LEDs, begin in the center and work outward. You can then mount the LED board onto the top of the PCB (printed-circuit board). See the online version of this Design Idea at www.edn.com/100624dic for photos, a parts list, and a video of this circuit in action.

To add the finishing touches to your project, use a small picture frame and in-

stall waxed paper onto the inside of the glass. Mount the LED board ¹/₄ to 1 in. away. The magnifying lens of the LEDs will produce a beautiful effect when they shine through the waxed paper.EDN



Figure 2 The LED in the center lights first, and the light then moves outward until the circuit products an 8×8-LED display.