Programmable audio attenuator

Gain controlled line amplifier offers a 60 dB range in 1 dB steps

by J. M. Didden

After experimenting with various linear gain control systems, the author chose a combination of linear and logic circuits to provide a high quality audio attenuator. The final design uses a 6-bit word to program the gain, and can be used for remote control applications or, with the aid of a microprocessor, for automatic level control.

This circuit was originally designed to remotely control the volume and balance in a stereo system. Several methods were tried, such as the two-quadrant multiplier in Fig.1. However, this circuit suffered from high distortion for input levels of more than 100mV, and tracking between units was poor. Attempts to improve the performance with current-source loading did not significantly improve the performance. A f.e.t. used as a voltage controlled resistor produced similar problems, so a l.d.r. design was tried as shown in Fig.2.

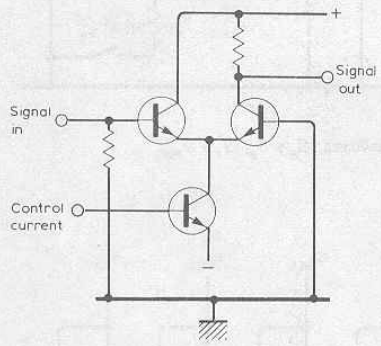

Fig. 1 Basic two-quadrant multiplier.

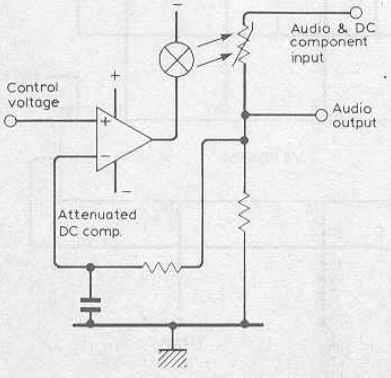

Fig. 2 Closed-loop light dependent resistor attenuator.

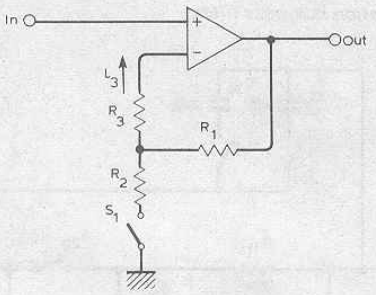

Fig. 3 Basic gain switching circuit.

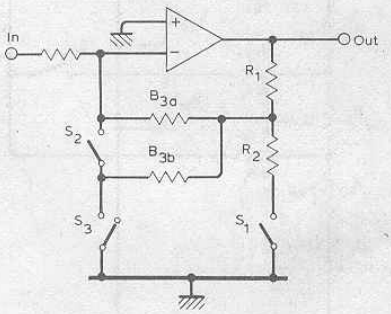

Fig. 4 Extended circuit with two independent switches.

This circuit had a good signal level capability, and tracking between units was made almost perfect by using a compound audio plus d.c. input. The attenuated d.c. was fed back to the control circuit. Unfortunately, the l.d.r. produced high noise levels at medium to high attenuation, and control-loop stability was difficult to achieve. Because these analogue approaches did not produce the performance required, I investigated gain switching with f.e.ts. Although f.e.ts are nonlinear, this is not a problem if the signal voltage across a closed switch is very small. A basic circuit is shown in Fig.3. When f.e.t. S_1 is closed, the signal across it equals the input voltage times the ratio of the f.e.t. on resistance to R_2. In practice, ratios of 1/1000 are easily obtained, so a signal level of several volts, which is not uncommon in a line amplifier, produces only a few millivolts across the switch. At these levels the f.e.t. is almost perfectly linear. Two independent gain settings can be achieved by switching R_3 and keeping I_3 constant. With S_2 closed and S_3 open in Fig.4, R_{3a} and R_{3b} are connected from R_1 to the virtual earth of the op-amp. With S_2 open and S_3 closed, R_{3b} is connected to the real earth. Therefore, by using a s.p.d.t. switch for S_2 S_3, and a s.p.s.t. for S_1, four gain settings are possible.

An extension of this circuit is shown in Fig. 5 where, with S_5 closed and S_4 open, gain is determined by the ratio of R_5 to R_1. With S_5 open and S_4 closed, the gain is determined by the ratio of R_5 to R_1 and R_3 to R_4. Combining the circuits in Fig. 4 and Fig. 5 gives eight gain settings. For all of these configurations the switches have only a small signal across their on resistance and carry very little current when opened. The values of the series resistors are high compared with the off resistance.

Selection of a suitable f.e.t. presented some problems. Switch arrays for analogue applications are available, but are generally expensive. Analogue multiplexers, such as the 4051, contain eight c.m.o.s. switches with a common input and integral one-of-eight decoder for control by a 3-bit word. However, the switching produces spikes on the audio output due to an internal capacitive coupling of the control signal to the switch terminals. This can be minimised by loading the switch, but smaller resistors must then be used which consequently produces higher distortion levels. Although "soft" switching with a RC network is one solution, see Fig. 6,

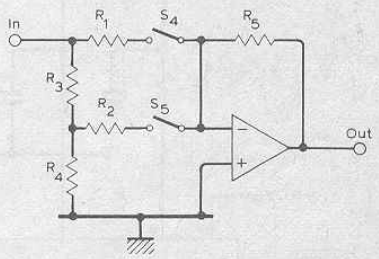

Fig. 5 Alternative two-switch circuit.

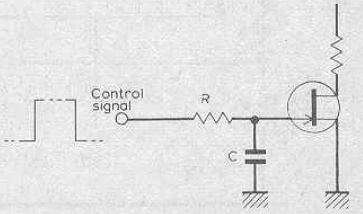

Fig. 6 Soft switching to overcome spikes.

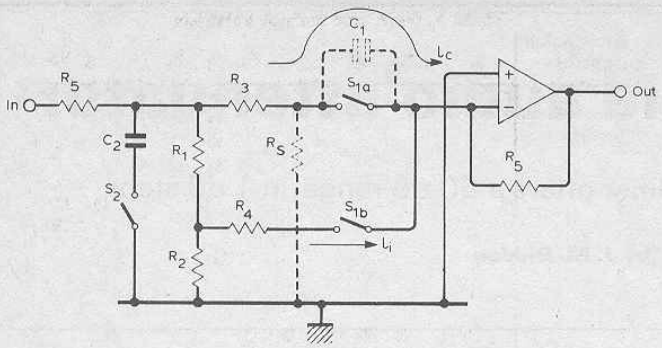

Fig. 7 Internal capacitance effect and compensation low-pass filter.

the gate of the f.e.t. must be accessible. I finally decided to use the low cost 4007 which contains two s.p.d.t. switches and an inverter.

In practice, 1dB steps in gain produce a gradual change and a range of about 60dB is sufficient for most applications. Because high value series resistors are required, high attenuation can only be achieved with the circuit in Fig. 5. However, as shown in Fig. 7, if S_{1b} is closed and S_{1a} is open, a small current flows through the internal switch capacitance. At high attenuation and high signal frequencies, this current may not be insignificant and can cause an output that rises with frequency.

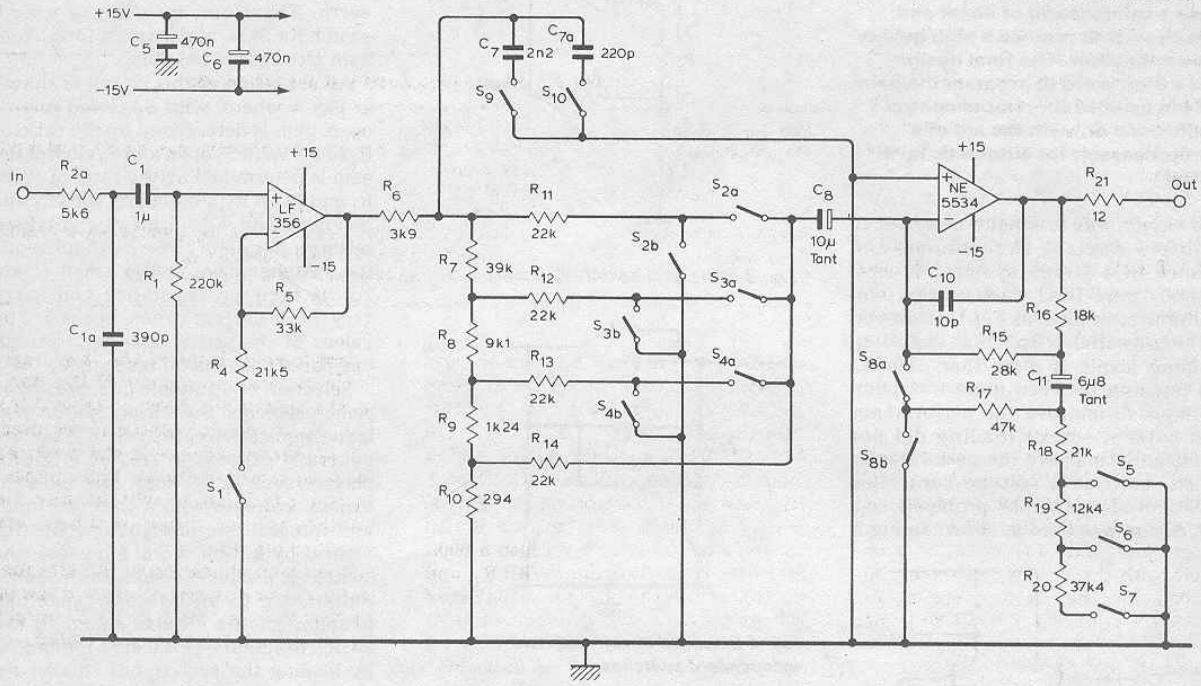

Fig. 8 Complete attenuator circuit for one channel. The switches are grouped in five i.cs as follows; S_5+S_6, S_7+S_{8ab}, $S_{2ab}+S_{3ab}$, $S_{4ab}+S_1$ and S_9+S_{10}. All resistors should be 1%.

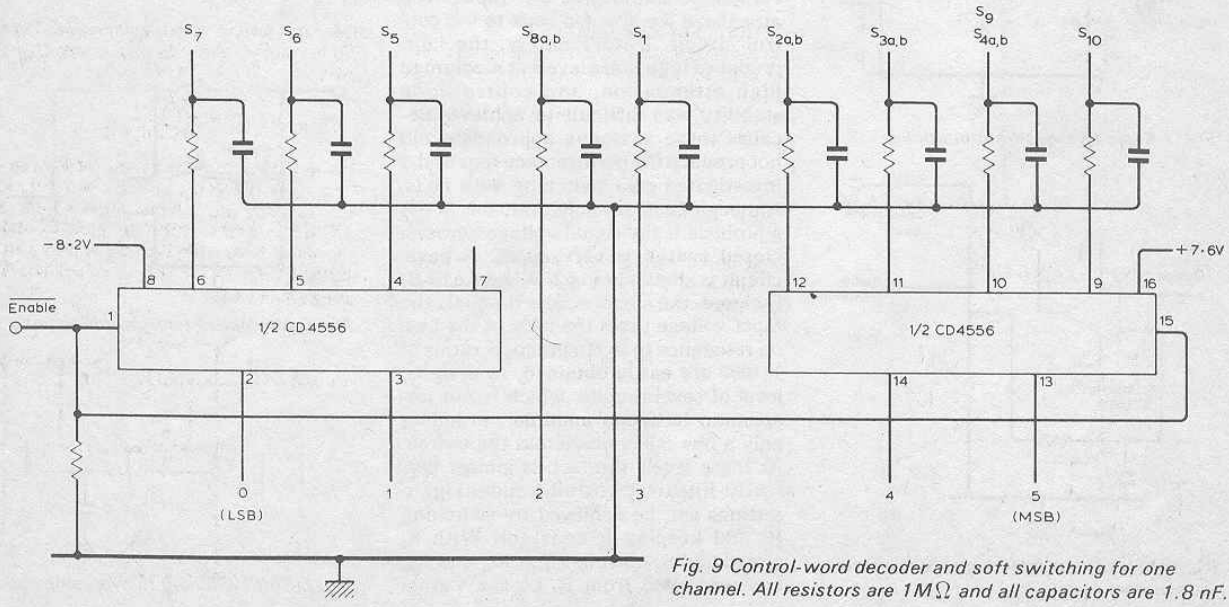

Fig. 9 Control-word decoder and soft switching for one channel. All resistors are 1MΩ and all capacitors are 1.8 nF.

This problem can be overcome by grounding the left terminal of S_1 when it is open, and this is easily achieved with the 4007 s.p.d.t. switches. Because there is an on resistance, R_s, a small signal voltage remains across the open switch. The low-pass filter R_5 C_2 compensates for this with S_2 closed when S_{1b} is closed and S_{1a} is open. The frequency response is flat within 0.3 dB up to 25 kHz and at high attenuation. Fig. 8 shows the final circuit for one channel and table 1 shows the range of attenuation levels. Ten mixed s.p.s.t. and s.p.d.t. switches are required and these can be produced with five 4007 i.cs. It is important that the signal amplitudes across S_1, S_8, S_5, S_6 and S_7 do not exceed the positive or negative supply voltages because an internal protection diode will conduct and cause distortion. As audio signals are bipolar, the supply voltage should be centered around ground because one side of the open switches is always connected to either a signal ground or virtual earth. To balance the on resistances of the p and n-channel m.o.s.f.e.ts, a positive supply of 7.6V and a negative supply of 8.2V is used. In Fig. 8, S_1 and $S_{8a,b}$ can be controlled by a single bit. Switches S_{2a} to S_{4b} and S_5 to S_7 require the four decoded values of a 2-bit control word. This is carried out by a 4556, which containes two one-of-four decoders, see Fig. 9.

Selection of the switch-network resistors is a compromise as already explained. The typical on resistance of a switch is about 300Ω and the maximum variation is about 200Ω. With a series resistor of 22kΩ 1%, this is comparable with the switch tolerance. Calculations for the resistor values are given in the appendix. Fig. 8 also shows that some switches are capacitor-coupled to the circuit by C_8 and C_{11}. These remove a small output offset-voltage change with gain which can be heard as clicks at low input signal levels.

The capacitor values have been chosen to give a low-frequency response to below 10Hz. A f.e.t. input op-amp, LF 356, is used to provide a high input impedance, wide bandwidth, high slew-rate and low distortion. A NE 5534 is used at the output because it can deliver a high output level into a 600Ω load with little distortion. With R_{21} and C_{10} to stabilize the op-amp, a 10nF load will not produce ringing or overshoot of a square-wave signal. The 5534 is also a low noise device, which is important, because most of the attenuation takes place at its input and this reduces the signal-to-noise ratio of the last stage. Performance parameters of the complete amplifier are shown in table 2. If a f.e.t. input selector switch is required, the LF 350 can be used in the inverting mode as shown in Fig. 10. The compensation capacitors, which may be necessary with other op-amps, are shown in Fig. 11.

If a visual indication of the attenuation is required, the control word can be converted to a two-digit b.c.d. output for driving a seven segment display.

To be continued

Table 1. Gain and switch settings

Attenuation steps dB	S_1	S_{2a}	S_{2b}	S_{3a}	S_{3b}	S_{4a}	S_{4b}	S_5	S_6	S_7	S_{8a}	S_{8b}
0								C	O	O		
1								O	C	O		
2								O	O	C		
3								O	O	O		
0											O	C
4											C	O
0	C											
8	O											
0		C	O	O	C	O	C					
16		O	C	C	O	O	C					
32		O	C	O	C	C	O					
48		O	C	O	C	O	C					

Table 2. Performance details of the attenuator

Max. r.m.s. output level	8.5V across 600Ω.
Max. input level	3.8V or 9V depending on S_1, provided max. output level is not exceeded.
Max. capacitive load	10 nF.
Frequency response	better than 10 Hz to 25 kHz within 1 dB.
Output noise level	at least 86 dB below 1 V r.m.s. at all gain settings (unweighted).
T.h.d. and i.m.	less than 0.03% and 0.02% respectively.
Gain	variable in 1 dB steps from 16.8 dB to −46.2 dB.

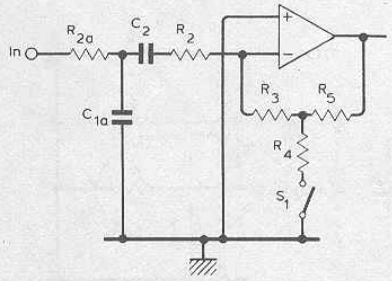

Fig. 10 Inverting input buffer.

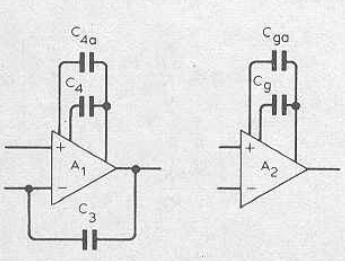

Fig. 11 Alternative compensation networks for other op-amps.

Appendix

Calculation of resistor values.
For these calculations a dB table or calculator with log. and inverse log. functions is required.
For the 1, 2 and 3 dB attenuators in Fig. 12, with S open,

$$i = \frac{U_{u1}}{R_1 + R_f} \qquad (1)$$

for an output of U_{u1} volts. With S closed and an output of U_{u2} volts, the equivalent voltage source U_1 is

$$U_{u2}\frac{R_x}{R_1 + R_x} \qquad (2)$$

and the equivalent source resistor is

$$\frac{R_1 R_x}{R_1 + R_x} \qquad (3)$$

therefore,

$$i = U_{u2}\frac{R_x(R_1 + R_f)}{R_1 R_x + R_f(R_1 + R_x)} \qquad (4)$$

Because i always equals i_s, equations (1) and (4) are equal. Substituting G for U_{u2}/U_{u1} gives

$$R_x = \frac{R_1 R_f}{(G\text{-}1)R_1 + R_f} \qquad (5)$$

The minimum resistor values for R_1 and R_f, for a given G and R_x, are obtained if $R_1 = R_f$. The minimum R_x is found for $G = 3$ dB and, taking $R_x = 20$kΩ as a design value, R_1 and R_x are about 18kΩ. However, R_f is also part of the 4dB network, so this is calculated first using a R_f of 18kΩ.

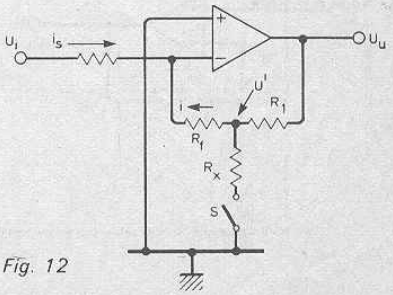

Fig. 12

The circuit is given in Fig. 13. If S_1 is closed and S_2 is open,

$$i=\frac{U_1}{R_1}+\frac{U_1}{R_2} \quad (6)$$

With S_1 open and S_2 closed,

$$i=\frac{U_1}{R_1} \quad (7)$$

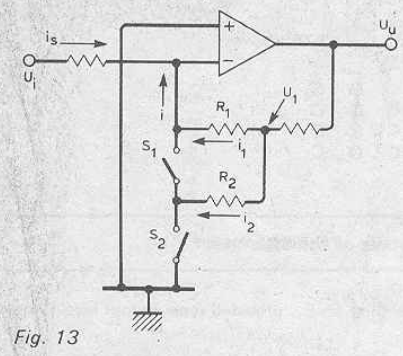

Fig. 13

As already mentioned, i_1, i_2 and U_1 are equal in both cases. In the first case, gain is the ratio of i_s to i_1+i_2, and in the second case, the ratio of i_s to i_1. The change in gain is therefore

$$G=\frac{i_1+i_2}{i_1} \quad (8)$$

and equations (6), (7) and (8) give

$$R_1=R_2(G-1) \quad (9)$$

and

$$R_2=\frac{R_1}{G-1} \quad (10)$$

Substituting $R_1//R_2=18\text{k}\Omega$ in (10) gives

$$R_2=\frac{G.18\text{k}\Omega}{G-1} \quad (11)$$

For $G=4$dB, R_2 is about 48kΩ. Using the standard value of 47kΩ and adding the nominal on resistance of the switch gives 47.3kΩ and R_1 becomes 27.6kΩ. With the nearest preferred values, R_{15} is 47kΩ and R_{17} is 28kΩ in Fig. 8.

The value of R_f in (5) now becomes 17.46 kΩ, i.e. $R_1//R_2$. The R_x values are calculated next.

For $G=1$ dB, R_x is 72.64 kΩ, which is the on resistance in Fig. 8. For $G=2$ dB, R_x is 34.23 kΩ which is $R_{18}+R_{19}+$ on resistance. For $G=3$ dB, R_x is 21.48 kΩ, i.e. $R_{18}+$ on resistance. With the nearest preferred value, R_{18} is 21 kΩ, R_{19} is 12.4 kΩ and R_{20} is 37.4 kΩ.

For the 8 dB switch refer to Fig. 14. With S open the gain is 0 dB, and with S closed the gain is R_1+R_x/R_x which gives

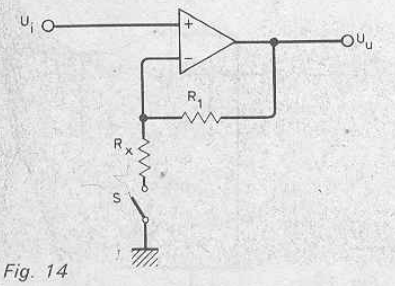

Fig. 14

$$R_x=\frac{R_1}{G-1} \quad (12)$$

Choosing 33 kΩ for R_1 gives 21.83 kΩ for R_x. Subtracting the 300Ω on resistance gives a standard value for R_4 in Fig. 8 of 21.5 kΩ and 33 kΩ for R_5.

Calculations for the remaining switch network are more difficult because the series resistors are either connected to ground or to virtual earth, see the equivalent circuit in Fig. 15. To save a switch, R_{14} in Fig. 8 always

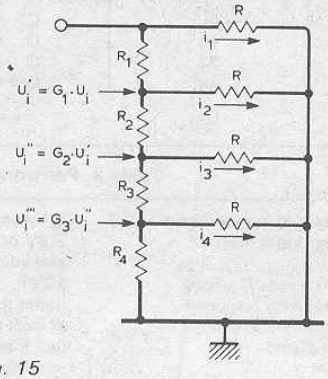

Fig. 15

delivers current to the summing node. Therefore, for the various gain settings, the following input currents flow;

No attenuation, i_1+i_4

−16 dB, i_2+i_4

−32 dB, i_3+i_4

−48 dB, i_4

For a gain step A, the current ratios are

$$A=\frac{i_2+i_y}{i_1+i_y} \quad (13)$$

$$A=\frac{i_3+i_y}{i_2+i_y} \quad (14)$$

$$A=\frac{i_y}{i_3+i_y} \quad (15)$$

If all series resistors are equal, gain changes only depend on voltages G_1U_i, G_2U_i and G_3U_i. Therefore,

$$G_1=\frac{i_2}{i_1} \quad (16)$$

$$G_2=\frac{i_3}{i_2} \quad (17)$$

$$G_3=\frac{i_4}{i_3} \quad (18)$$

If A is −16dB,

$$G_3=\frac{A}{1-A}(0.188-14.5\text{dB}) \quad (19)$$

$$G_2=\frac{A}{1+A}(0.137-17.3\text{dB}) \quad (20)$$

$$G_1=\frac{A}{1+\frac{A^2}{1+A}}(0.155-16.2\text{dB}) \quad (21)$$

Note that A is the input-current gain step and G_n is the gain step of the voltage across the series resistor relative to G_n-1.

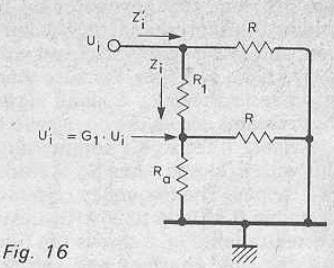

Fig. 16

In the simplified circuit of Fig. 16, because $Z_i^1 = Z_i//R$,

$$Z_i=\frac{Z_i^1 R}{R-Z_i^1} \quad (22)$$

and

$$R_1=Z_i\frac{R \cdot R_a}{R+R_a} \quad (23)$$

also, because

$$G_1=\frac{\frac{R \cdot R_a}{R+R_a}}{Z_i}$$

$$G_1Z_i=\frac{R \cdot R_a}{R+R_a}$$

Therefore,

$$R_1=Z_i(1-G_1) \quad (24)$$

and

$$R_a=\frac{R \cdot G_1 \cdot Z_i}{R-G_1 \cdot Z_i} \quad (25)$$

Again, using a design value of 22kΩ for the series resistors, and adding 300Ω on resistance gives 22.3 kΩ for each resistor. As R_{14} in Fig. 8 has no series switch, R in formula (30) and on will be 22 kΩ. After a little trial-and-error to find a standard value for R_1, the value of Z_i^1 was set to 15.04 kΩ, which is the constant load presented to the buffer amplifier. From (22), (23) and (24), Z_i is 41.2 kΩ and R_1 is 39 kΩ. From (25), R_a is 10.55 kΩ. By repeating this procedure Fig. 17 is achieved where

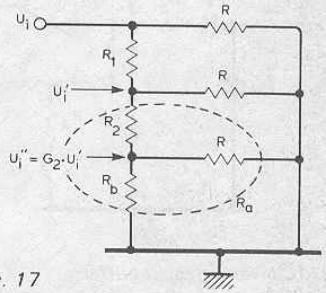

Fig. 17

$$R_2=R_a-\frac{R \cdot R_b}{R+R_b} \quad (26)$$

$$G_2=\frac{\frac{R \cdot R_b}{R+R_b}}{R_a} \quad (27)$$

continued on page 74

burst of 3, making a total of 43 (including the no-error case). The first cyclic burst-error-correcting codes, due to P. Fire, needed $3b - 1$ check digits for bursts of length up to b, but later codes listed by Lucky, Salz and Weldon[7] are better. Peterson and Weldon quote on p.364 a code length 15 capable of correcting bursts up to length 3 with only 6 check digits, as against 10 or 3 random errors. In fact the rule is that a code capable of *detecting* bursts up to length b needs precisely b check digits but a code for *correcting* such bursts needs *at least* $2b$ check digits. Codes using exactly $2b$ check digits are known for lengths 7, 15, 27, 34 and 50 with corresponding values of b of 2, 3, 5, 6 and 8; and a few more check digits are required for longer codes. (But the longer codes cited by Peterson and Weldon have mostly fairly small values of b, between 3 and 7).

The mathematical techniques used in the construction of these cyclic burst-error-correcting codes are very similar to those of the BCH codes. For example the (15,9,3b) code for correcting bursts up to length 3 can be constructed from the pattern

1 1 1 1 0 0 1 0 0 0 0 0 0 0 0

which is taken to be 2^8, and its 8 right shifts which are taken to be the powers of two from 2^7 to $2^0 = 1$. Then the decimal number 409, which is $2^8 + 2^7 + 2^4 + 2^3 + 2^0$, encodes as

1 0 0 0 0 0 1 1 0 1 0 0 0 0 1

There may be a requirement to correct both random and burst errors. It is often said that random errors are typical of radio communication, as a result of thermal and shot noise in the receiver and atmospherics; but bursts are typical of land-line circuits, as a result of intermittent contacts in switching systems or interference from power lines. But clearly this is an oversimplification, particularly as land lines are using higher and higher frequencies, to say nothing of wave guides and optical fibres. Then one device to avoid special measures for the correction of burst errors as well as random errors is to scramble the order of digits before transmission and unscramble them at the receiver. The re-ordering of digits at the receiver will break up any bursts into scattered errors which can be dealt with by a code for random errors. However, the whole point of burst-error-correcting codes is that for a given number of check digits they can deal with more errors in a burst than scattered at random; so the scrambling should extend over more than one block so that, for example, a burst of 6 errors in one block length during transmission becomes 3 random errors in each of two blocks after "unscrambling" in the receiver.

Error-correcting and error-detecting codes constitute a vast subject, with special codes being developed for special purposes. This article makes no pretence of reviewing the subject: it aims merely to explain some of the underlying principles with illustrative examples. The subject is formidably mathematical, so that most users will be content to use existing codes rather than attempt to design codes for themselves; but even to list all existing codes with their properties would be a very major undertaking. Most of them can be found in books such as Peterson and Weldon[4] but there are always a few which have been developed since the publication of a book. Fortunately the basic codes such as BCH will serve for most purposes.

Appendix. The Golay code

Golay discovered a triple-error-correcting binary code of length 23, with 12 information digits, which is perfectly packed. A code of length $n = 23$ and capable of correcting up to 3 random errors will have to be able to distinguish between $1 + 23 + \binom{23}{2} + \binom{23}{3}$ error patterns. The binomial coefficients evaluate to 253 and 1771 so that the whole series sums to 2048, which is exactly 2^{11}; and so with 11 check digits (and therefore 12 information digits) the code is perfectly packed. This Golay (23,12,3) code is the only binary code capable of correcting more than one error which is perfectly packed. A cyclic code which is equivalent to the Golay code can be developed from the following sequence and its eleven shifts:–

1 0 1 0 1 1 1 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0

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From this

$$R_2 = R_a(1-G_2) \qquad (28)$$

and

$$R_b = \frac{G_2 R_a R}{R - G_2 R_a} \qquad (29)$$

Therefore, R_2 is 9.09 kΩ (9.1 kΩ standard value) and R_b is 1.54 kΩ. The last step gives Fig. 18 where

$$R_3 = R_b - \frac{R \,.\, R_y}{R + R_y} \qquad (30)$$

and

$$G_3 = \frac{\dfrac{R \,.\, R_y}{R + R_y}}{R_b} \qquad (31)$$

From (30) and (31),

$$R_3 = R_b(1-G_3)$$

and

$$R_y = \frac{G_3 \,.\, R_b \,.\, R}{R - G_3 \,.\, R_b}$$

The nearest standard value for R_3 is 1.24 kΩ and for R_4 is 294Ω. These calculations give an idea of the accuracy that can be expected. The worst case error occurs with a maximum error in the input switching network of A_2. If, for example, R_{11} and S_{2a} in Fig. 8 each have a maximum resistance error of 200Ω in the same direction, the gain error would be no more than 0.15 dB.

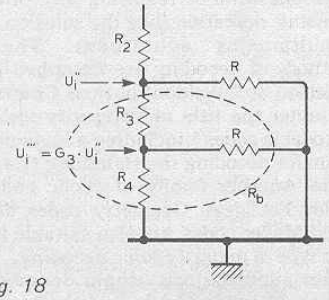

Fig. 18

Printed circuit board

A printed circuit board which accommodates one attenuator circuit and decoder will be available for £4.20 inclusive of v.a.t. and UK postage from M. R. Sagin at 23 Keyes Road, London NW2.

The author

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The author is currently involved with software design for NATO air defence systems. Apart from audio, his hobbies include reading science fiction.